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Magnetic Graphene Memory Circuit Characterization And Verilog-A Modeling

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MAGNETIC GRAPHENE MEMORY CIRCUIT CHARACTERIZATION AND VERILOG-A MODELING

A Thesis Presented

by

Greg Abrami

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ABSTRACT

Memory design plays an important role in modern computer technology in regard to overall performance and reliability. Prior memory technologies, including magnetic-core memory, hard disk drives, DRAM, SRAM have limitations in regard to bit density, IC integration, power efficiency, and physical size, respectively. To address these limitations we propose to develop a magnetic graphene random access memory (MGRAM) utilizing graphene Hall effect, which takes advantage of the inherent reliability of magnetic memory and superior electrical properties of graphene (high carrier mobility, zero-band gap, high Hall sensitivity). As the graphene magnetic memory device will be integrated with a CMOS ASIC design an analog circuit model for the MGRAM cell is necessary and important. In this study the electrical circuit model is developed utilizing the analog circuit modeling language Verilog-A.

The electrical circuit model characterizes the graphene electrical properties and the ferromagnetic core magnetic properties that retains the bit-state value. MGRAM device simulations studying varying coil width, height, radius, contact pad configuration, graphene shape, is performed with the MagOasis Magsimus tool to evaluate the device performance. Model results show a maximum Hall effect voltage of 100mV for a bias current of 50uA with a 1 Tesla magnetic field, and a writing speed of 6-9ns for setting the magnetic state. These results will be validated against the circuit hardware measurement and will be used for model refinement.
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CHAPTER 1: INTRODUCTION & PROJECT OVERVIEW

1.1. Prior Art

In this section, a general review of computer memory and its operation within a computer system will be introduced. General semi-conductor memory categories will also be discussed along with a type of memory for each category. Each memory type will be described in length about how it operates and its limitations. Memory is a vital component in modern digital computing systems. A memory cell is a single device that stores one bit of information and an array of memory cells constitutes a memory unit. A memory unit’s size is determined by the number of bits it can store, typically denoted by a byte unit which is eight bits.

The two main semi-conductor memories that will be discussed are random access memory (RAM) and read only memory (ROM). A memory falls in the RAM category if the memory cells are readable and writeable. A memory falls in the ROM category if the memory cells are read only access, or a limited write access. Generally RAM is a volatile memory, meaning when power is removed all storage of information is lost. While ROM is a non-volatile memory, meaning it retains information even when power is removed.

Static random access memory (SRAM) is a memory device typically consisting of six transistors per cell (bit) (Fig. 1) and is a common choice for integrated chip (IC) designers. The memory array physical architecture is a cell grid with rows and columns where an entire row, column, or a single cell can be accessed for a read or write operation. Read and write access is performed by setting the word line and bit line voltages. A typical SRAM cell (Fig. 1) stores a bit value by looping two inverters together (MN2/MP2 and MN1/MP1). The Q and Q’ bit states remain steady as long as the word line (WL) remains
low (i.e. 0 V) and thus transistors MB & MA are off. Since the cell is static it draws very little current, only the quiescent/leakage current is present while holding the Q/Q’ bit states. Holding the value requires a constant gate voltage on the MN1/MN2/MP1/MP2 transistors and thus a leakage current is always present in a SRAM cell. Power consumption of a SRAM cell is very low outside of a read or write operation.

Writing to the cell is performed by applying the word line to a high voltage, thus turning on MB and MA, and applying the bit line (D & D’ in Fig. 1) to the desired stored value. The inverter loop captures and stores the data. Reading the cell is performed by first using pull-up transistors (MP3/MP4) to pre-charge the bit lines. Then applying the word line high to turn on MB and MA. The bit line or the bit line complement will drain into whichever Q node holds the low (relatively zero voltage) value. A voltage delta between the bit lines will be produced that can be sensed by the peripheral sense circuitry.

An inherent DC power component is present in SRAM cells, while the MN1/MN2/MP1/MP2 inverter loop is holding the bit value a quiescent current leakage adds to the total power usage. SRAM is a volatile memory device, when power VDD is removed the MN1/MN2/MP1/MP2 inverter loop no longer can maintain the bit value. In addition, reliability issues during operation concerning parity errors drive array redundancy and error correction code development. Hard parity errors can arise from manufacturing defects and can be screened out during initial testing of the device. Soft parity errors are typically induced by radiation and require error correction code to resolve Ref. [20].
Dynamic random access memory (DRAM) is a memory device consisting of a single transistor and capacitor. DRAM has excellent bit density since its cell size in ICs is very small. The read and write operation are handled by a bit line and a word line to access a column and row, respectively, of a DRAM memory array. The physical architecture of DRAM is a cell grid with rows and columns, where an entire row, column, or a single cell address can be accessed. A read or write operation is performed by setting the word line and bit line high or low. Typically these operations are performed on a byte size. The cell bit value is stored by a capacitor (Fig. 2) which holds a charge for storing a ‘1’ and contains no charge when storing a ‘0’. A read operation is performed by applying a high value (voltage) to the word line turning on the transistor and the charge (if bit value is ‘1’) flows into the bit line to be sensed. If enough charge is present the bit line will read a ‘1’ otherwise it will read a ‘0’. An inherent issue with DRAM cells is that they must rely on the stored charge in the capacitor to drive the bit line. The discharge time makes DRAM,
relatively, a slower device overall. Also, DRAM read operations use the stored charge and thus all read cycles of a ‘1’ are followed by a write cycle to replenish the charge.

A write operation is performed by applying the word line high, which turns on the transistor, and applying the bit line to the desired stored value. If the bit line is high it will charge the capacitor (‘1’ bit value) or if it is low it will drain any charge in the capacitor (‘0’ bit value). An inherent issue with DRAM is that the capacitor will not statically hold the charge (volatile) and will discharge through the transistor quiescently (dynamic aspect) due to leakage current. The time for the capacitor to discharge is called its retention time. Thus all DRAM cells have a refresh rate (time constant) at which the charge in the capacitor needs to be restored. The leaking of the capacitor charge through the FET make DRAM thermally sensitive. Since the leakage current will increase with temperature, the upper thermal limit of the circuit is thus less than other memory devices.

Figure 2: DRAM Cell Ref. [11]
DRAM is a volatile device, like SRAM, when power is removed the information stored is lost. As mentioned this occurs even while the memory chip has power and a periodic refresh charge must be given to the cell. The temperature effect on the retention time of the DRAM cell is a 39.2% reduction per 10°C in most cases and worst case it is a 46.5% reduction per 10°C Ref. [21].

Flash memory (array of NAND or NOR gates) is a popular ROM semiconductor memory and used in solid state drives and portable thumb drives. Specifically, it is EEPROM (Electronically Erasable Programmable Read Only Memory). The initial ROM devices were strictly read only, such as mask ROM, which imprinted the memory on an IC during fabrication making it immutable and non-volatile. Mask ROM technology was followed sequentially by PROM (Programmable ROM), EPROM (Erasable PROM), and EEPROM. Each generation of ROM technology improved functionality. PROM (fuse devices) have a one-time write operation after fabrication with a high programming voltage. The high voltage breaks down the oxide between a gate and substrate material creating a permanent conductive channel. EPROM, with a floating gate, charges via hot carrier injection and dissipates charge via UV-light induced ionization. EEPROM uses electrically field induced Fowler-Nordheim tunneling to set the bit-state to zero. EEPROM has a faster read cycle than write cycle for individual cells; Flash memory performs write operations in page units to improve write speed. Flash memory has a program/erasure endurance limit of 10,000 cycles (for 30-40nm NAND), the cycle limit is expected to degrade further for subsequent technology nodes Ref. [22].
1.2 MGRAM Device and Modeling

This thesis will report analysis and modeling of a unique new magnetic memory device using a ferromagnetic core wrapped by coil structure and a graphene Hall cross. We propose to develop a magnetic graphene random access memory (MGRAM) utilizing the graphene Hall effect, which takes advantage of the inherent reliability of magnetic memory and superior electrical properties of graphene (high carrier mobility, zero-band gap, high Hall coefficient).

Graphene is a well-suited Hall material given its unique electro-magnetic properties (integer quantum Hall effect, zero-band gap). RF graphene transistors have been developed due to for its high carrier mobility. For example, in Ref. [20], 100 GHz transistors have been achieved with a gate length of 240 nm.

The device feature size of 100 nm allows package integration with peripheral CMOS ICs so as to develop a high density non-volatile magnetic memory chip. An accurate electrical model would therefore be indispensable to characterize the device and facilitate ASIC (Application Specific Integrated Circuit) design and simulation. For modeling, the device is treated as an analog circuit component and Verilog-A modeling language is utilized. The Verilog-A model is developed based upon graphene’s physical properties related to the Hall effect (carrier mobility, carrier density, gate voltage bias, chemical neutral point also known as the Dirac point), the coil’s structure and bias current, and the magnetic field from the ferromagnetic core.

The electrical circuit model characterizes the graphene electrical properties and the ferromagnetic core magnetic properties that retain the bit-state value in a non-volatile manner. MGRAM device performance is evaluated with the MagOasis Magsimus
simulator by studying effects of varying coil width, height, radius, and coil contact pad configuration.

1.3 Device Fundamentals

The magnetic graphene random access memory (MGRAM) device holds a bit state by the polarity of a ferromagnetic cylinder core in the center of a single loop coil. Fig. 3 shows the 3D structure of the MGRAM cell, comprising of the ferromagnetic core (dark blue), coil (brown) with contact pads, and the graphene Hall cross (light blue) on top of a substrate (red).

![Figure 3: 3D Structural Diagram of Graphene Hall Effect Memory](image)

![Figure 4: 2D Structural Diagram of Graphene Hall Effect Memory](image)
Fig. 4 shows the 2D MGRAM structure from the front (left) and top (right) perspectives, the core is centered directly over the middle of the graphene Hall cross. The substrate on the left is 300nm thick. The schematic diagram of the MGRAM cell shown in Fig. 5 is in a testing setup, which includes periphery components for pulsing write and read cycles.

The state/polarity can be set (write operation) by pulsing current through the coil. According to the right hand rule, the current flow through the coil induces a magnetic field which sets the polarity of the ferromagnetic core. The bit-state value of the ferromagnetic core, once set to an up or down direction (‘1’ or ‘0’), will be preserved in a non-volatile manner. Being non-volatile gives MGRAM an important quality in relation to other RAM devices. Also the device does not have an endurance limit of read/write cycles such as Flash memory.
The read operation is performed by current biasing an arm section of the graphene cross centered at the bottom of the ferromagnetic core, which produces a sensible transverse Hall voltage. The Hall voltage is proportional to the perpendicular magnetic field generated from the ferromagnetic core. Graphene’s electric properties give MGRAM potential for a fast read operation compared to other memories. An enhanced read speed is possible by a higher Hall sensitivity of graphene than silicon Ref. [2,9]. Graphene has a high carrier mobility up to 200,000 cm²/Vs Ref. [6] and its charge carriers that behave like mass-less fermions travel at a fraction of light speed (c/300) Ref. [1,3]. These characteristics improve the voltage sensing of the Hall device using graphene. Moreover, the graphene devices are thermally stable across a wide temperature range Ref. [2].

The thermal stability of the Hall effect read operation in MGRAM is a performance improvement compared to the relatively thermally sensitive read operation of DRAM. It is well known that DRAM retention time greatly reduces at high temperature and thus it is thermal sensitive Ref. [21]. DRAM memory modules used in server systems are rated for 85°C. When the temperature rises to 95°C and higher the, its reliability decreases. Processor speed must be throttled to prevent data fault incursion Ref. [17]. The temperature limit of 95°C hinders chip performance and reliability. Modern multi-core processors used in server systems contain dense circuitry. Thermal concentration follows with circuit density, hence an improvement of thermal stability of devices within the chip must also occur to maintain performance. In fact, chip manufacturers shipping modules (packaged ICs: multicore processors, memory chips, etc) that contain DRAM generally test the memory device at an elevated temperature to weed out weak DRAM cells. If a computer chip (i.e. module) containing DRAM fails this high temperature test either
memory redundancy must be used or the chip is removed from the shippable good list. In either case, cost and resources increase. The use of graphene in MGRAM and how it improves read operation thermal stability are discussed in section 2.4.

1.4 Research Objectives

MGRAM memory device performance will be assessed through published works on the electrical properties of graphene (Hall effect, quantum effects, high carrier mobility) and ferromagnetic materials. Simulation study of the device will be performed utilizing MagOasis Magsimus tool (which uses finite element numerical analysis at semiconductor scales), specifically on the optimal structure of ferromagnetic core and coil. An electrical circuit analytical model will then be developed in Verilog-A code that is applicable in typical integrated circuit design software (i.e. Cadence IC design program).

Several technical issues will be examined: optimal device structure, coil structure, coil contact pad size and position, the maximum device Hall voltage, graphene structure and back-gate voltage charge tuning, hysteresis curve of a ferromagnetic core, Hall plate shape, read cycle via current or bias voltage. We will study the integer quantum Hall effect (IQHE) in graphene and its applicability in a MGRAM cell. The MGRAM analytic model based on the Hall effect equations, dual charge carrier transport, and Biot-Savart law of induced magnetic field from a current-carrying coil, will be compared to simulation results obtained using MagOasis Magimus program.
CHAPTER 2: EDWIN HALL EFFECT

2.1 Hall Effect Fundamentals

In this section, the Hall effect basic principles are introduced, regarding the interacting effect between a current carrying medium in a magnetic field. Specifically the Lorentz force, Hall coefficient, and Hall voltage are discussed. Finally the fundamental Hall voltage equation is given.

The Hall effect, discovered by Edwin Hall in 1879, is resulted from the interaction of a transverse magnetic field upon a current carrying material. The Hall voltage is produced by such an interaction and is perpendicular to the current flow. The Hall effect has been a fundamental tool for over a century for measuring the conductivity and carrier mobility of a material. When current carriers (electrons or holes) move in a plane transverse to a magnetic field, the Lorentz force acts on them perpendicular to their motions. The Lorentz force diverts the charge carriers from their original path of the least resistance. A balancing electric field is created by the accumulation of charge on one side of the Hall material, which applies an equal and opposing force (to the Lorentz Force) on the charge carriers. The greater the Lorentz force the greater the electric field is generated. Thus by increasing the current or magnetic field flux, one can increase the induced electric field. Probing the perpendicular points of the plane on the Hall medium measures the Hall voltage that is proportional to the Hall coefficient, and inversely proportional to the density of charge carriers present. The Hall coefficient and Hall voltage are characteristics of the passive elemental nature of the Hall effect. The Hall effect does not generate power and only augments the flow of charge/current. The Hall effect has been utilized to develop many novel sensors, such as sensors that monitor a motor’s rotor position Ref. [23].
Figure 6: Hall Effect in a Rectangular Plate

The fundamental Hall voltage equation (Eq. 1) for a Hall plate characterizes the effects of plate thickness, charge carrier density, applied magnetic field, and current bias (voltage bias can replace current bias in any Hall voltage equation, but for the remainder of this thesis only current bias scenarios will be explored. The characteristic advantages of using bias current versus bias voltage will be discussed, please see Section 2.4). Fig. 6 shows a typical Hall rectangular plate with a transverse magnetic field, $B_y$, and a charge density, $J_x$. The charge carriers, electrons in Fig. 6(a) and holes in Fig. 6(b), have a Lorentz force ($F_z$) enacted on them in the positive $z$-axis direction. As the current flows parallel to the $x$-axis the carriers are skewed off their path towards the top of the plate. A perpendicular electrical field, $E_z$, is created in the $z$-axis direction as the result of a build-up charge. As the electrical field is formed, it creates a countering force on the charge carriers. The force of the electrical field on the charge carriers is equal to the Lorentz force. The Hall voltage can be characterized as [14]:

$$V_H = \frac{IB}{qnt} \quad (1)$$
The Hall voltage $V_H$ is determined by the applied current ($I$), transverse magnetic field ($B$), the plate thickness ($t$), and the charge density of the Hall material ($n$). Design applications of the Hall effect necessitate maximizing the Hall voltage. Increasing the magnetic field or current is not always applicable. The current contributes to power usage and the magnetic field strength may be fixed such as when the Hall effect is used as a compass Ref. [24]. Reducing the plate thickness or charge density of the material will lead to a greater Hall voltage.

While the fundamental Hall voltage is determined simply for a plate that is shaped as a very long rectangle, many other effects must be considered when dealing with different plate shapes. One effect to consider is the Hall angle, which is the angle at which an electron or hole is skewed off its’ original path by the Lorentz force. That Hall angle can be influenced by the Hall plate shape. Another effect determined by plate shape is the current flow, for instance the curved current flow in a Corbino disc.

### 2.2 Hall Plate and Shapes

In this section, different Hall plate shapes and how the different shapes can potentially decrease the Hall voltage by their geometric correction value are introduced. The shape of a Hall sensor is critical in producing a measurable Hall voltage. The geometric correction value, $G_C$, is added to the Hall voltage equation to account for the loss in voltage, Ref. [14]:

$$V_H = G_C \frac{IB}{qnt} \quad (2)$$
When $G_C$ approximately equals one it is removed from the above equation as it has a negligible effect on the output Hall voltage. It will be shown that a cross shape has an effective $G_C$ value of one, an infinitely long rectangle will also have no geometric correction in its Hall voltage equation. Eq. 3 shows the relationship between the length to width ratio and $G_C$ for the scenario of a rectangular Hall plate, where $W$ is the width of the plate and $L$ is the length, Ref. [14]:

$$
G_C = 1 - \frac{16}{\pi^2} e^{-\frac{\pi L}{2W}} \left( 1 - \frac{8}{9} e^{-\frac{\pi L}{2W}} \right) \left( 1 - \frac{\theta_H^2}{3} \right) \quad (3)
$$

The Hall angle, $\theta_H$, is the angle at which a charge carrier is deflected by the Lorentz force, which can be calculated based up the carrier mobility ($\mu$) and magnetic field ($B$) of the Hall cross, Ref. [14]:

$$
\theta_H = \mu B \quad (4)
$$

The maximum Hall angle is $\pi/2$, which when applied to Eq. 3 (with $W=L$), the geometric correction factor is close to unity ($G_C=0.951$). For smaller Hall angles, the rectangular Hall plate needs to employ the geometric correction factor in regard to the output Hall voltage. The material being considered in the MGRAM device is graphene, which has a relatively higher carrier mobility (5000 cm$^2$/Vs or greater) compared to other materials. Thus graphene would have a Hall angle approaching the maximum of $\pi/2$ even at low magnetic fields. The formula for the geometric correction of a Hall cross, Eq. 5, directly depends on the Hall angle. If the Hall angle is close to $\pi/2$ (as it is with graphene) then the group of terms on the right will approach zero. The geometric correction will approach unity and will not need to be included in the Hall voltage equation (Eq. 5), Ref. [14]:

$$
G_C = 1 - g(\lambda) \frac{\theta_H}{\tan \theta_H} \quad (5)
$$

14
The thickness of the material has an inverse relationship to the hall voltage, Ref. [14]:

\[ V_H = \frac{R_H B I}{t} \] (6)

The Hall voltage (Eq. 1 & 2) often is written with the Hall coefficient, \( R_H \), which will be referred to later as the Hall sensitivity. The Hall coefficient is indirectly proportional to the charge density.

### 2.3 CMOS Hall Sensor

In this section, the CMOS Hall sensor and how it is related to the graphene Hall effect in the MGRAM device are introduced. The MGRAM reading operation is performed by a graphene Hall cross with a semiconductor feature size of 100 nm which is comparable to the dimension of a CMOS Hall sensor. Examining its usage is important for the consideration of how a graphene Hall cross might operate.

![Cross Shaped CMOS Hall Sensor](image)

**Figure 7: Cross Shaped CMOS Hall Sensor Ref. [15]**
A CMOS Hall sensor will use doped silicon as the Hall material. With device back-gating, a higher charge carrier density can be achieved. There are numerous considerations when dealing with embedded CMOS Hall sensors. The sensor thickness will have an effect on the output Hall voltage. How to effectively create a uniformly shaped charge channel in the Hall material must be considered when using CMOS technology in Hall sensor designs. One technique to address charge channel uniformity is to use a top and bottom gate design. Typically the material is doped silicon as it is a standard material in CMOS fabrication. Fig. 7 shows an illustration of a CMOS Hall cross sensor. Varying thickness of the silicon complicates predicting and controlling the Hall sensitivity (Hall coefficient) Ref. [16, 17]. Additional techniques are employed to ensure accurate measurements, such as cross current pulsing (offset correction) to help balance the sensor Ref. [16, 17].

![Cross Section of CMOS Hall Sensor](image)

**Figure 8: Cross Section of CMOS Hall Sensor Ref. [16]**

CMOS Hall effect sensing chips employ multiple sensors to perform one measurement. For instance, a chip that measures the earth’s magnetic field (a Hall effect compass) can use four CMOS Hall sensors to accurately give the direction of magnetic
north. The cross section of a CMOS Hall sensor (Fig. 8) has an active area where a charge channel forms. When the channel is not uniform across the length of the sensor, the effective thickness of the charge channel varies accordingly. A varying thickness, caused by a back-bias & top-bias effect on the depletion zone Ref. [16], will increase the variability of the Hall voltage. The Hall effect in graphene is consistent due to a stable, non-varying charge channel. Graphene electron and hole carrier mobility is consistent throughout the material and varies very little with temperature Ref. [2].

2.4 Current and Voltage Bias

In this section, current and voltage bias of a Hall sensor and their effects on Hall sensor’s sensitivity (Hall coefficient) are discussed. The thermal insensitivity of a graphene Hall cross output voltage is also reviewed.

A Hall sensor can be either current biased or voltage biased. CMOS Hall sensors that are current biased are better suited for measuring magnetic fields as opposed to voltage biased devices due to the magnetoresistance effect. The magnetoresistance effect, which can occur in conjunction with the Hall effect, is caused by the Lorentz force on charge carriers. As discussed before, the Lorentz force is present on moving charge carriers (electrons and holes) in a magnetic field to cause a deflection in the current path. A deflection from the original straight path increases the total path of the charge carrier and effectively increases the resistance of the material. The effective resistance change is known as the magnetoresistance effect. A nonlinearity Hall voltage issue arises when voltage mode is employed Ref. [2]. Non-linear voltage output, varying by the magnetic field, reduces the accuracy of the Hall device. By using the Hall material in a current biased
read cycle, the consistency and reliability of the memory device improves. In addition, Graphene has thermally stable electrical properties in a wide temperature range, 1.8 – 400 K Ref. [2]. Hence it can be used in a Hall device for applications where temperature varies, i.e. aircraft.

![Graphene measured Hall Sensitivity versus Temperature Ref. [2]](image)

**Figure 9: Graphene measured Hall Sensitivity versus Temperature Ref. [2]**

As seen in Fig. 9(a) the Hall Voltage varies minutely, between 1.8 K and 100 K on the order of only 1% change in output. In Fig. 9(b) the data shows that 10% change in Hall sensitivity (which directly affects the Hall output voltage) occurs past 200 K.

### 2.5 Using Graphene as Hall Materials

In this section, the silicon and graphene Hall sensitivities are discussed and compared. A Hall material can be any conducting medium. The Hall effect is widely used to determine the conductivity of newly found materials. Several factors determine if a material is suitable to be used in a Hall effect sensor. Carrier mobility is a primary concern for an accurate Hall sensor and can alter the sensitivity of the material to an induced
magnetic field. Cost, manufacturability, and scalability (for integrated circuits) are second order concerns for a Hall effect material. Integrated circuits (IC) prevalently use doped silicon for creating Hall effect sensors. New research presented here shows the use of graphene as a Hall material in an IC design as a replacement to doped silicon. A transition from silicon to graphene, for a Hall material, improves the Hall coefficient and reduces the output Hall voltage noise. Silicon remains dominant as a Hall material because it is readily scalable and reliable throughout all semiconductor fabrication technology nodes.

A typical Hall coefficient (or sensitivity) of silicon is around 100 V/AT which is an order of magnitude lower than that of graphene Ref. [2]. Variation of silicon Hall sensitivity versus temperature is also an issue as shown in Fig. 10, whereas graphene Hall sensitivity variation versus temperature is very small. The use of graphene in the MGRAM device is a temperature and voltage performance improvement over silicon, which is a

**Figure 10: Hall Sensitivity Variation versus Temperature Ref. [9]**

A typical Hall coefficient (or sensitivity) of silicon is around 100 V/AT which is an order of magnitude lower than that of graphene Ref. [2]. Variation of silicon Hall sensitivity versus temperature is also an issue as shown in Fig. 10, whereas graphene Hall sensitivity variation versus temperature is very small. The use of graphene in the MGRAM device is a temperature and voltage performance improvement over silicon, which is a
widely used Hall material Ref. [14]. The graphene Hall effect gives the MGRAM device a higher potential performance ceiling, in regard to Hall sensitivity and thermal stability.
CHAPTER 3: GRAPHENE

3.1 Structure & Electrical Properties

In this section, graphene’s structure and electrical properties, and their effects on MGRAM device are introduced. Different graphene manufacturing techniques are also discussed. Graphene is a two dimensional material consisting in its pure form as a carbon honey-comb lattice. Graphene is classified as a ‘semi-metal’ as it exhibits qualities of a highly conductive metal born from its structure, while its band gap is not similar to a traditional metal’s bandgap. In conventional three dimensional metals, electrons move in the direction of an induced electric field. Before long the electrons will collide with an atom and then continue moving in the direction of the electric field lines until another collision occurs. The average time between these collisions is characterized as the scattering time. Scattering time determines the drift velocity which is a key electrical property of a traditional conductor. Electron and hole mobility is directly dependent on the drift velocity.

In graphene, electrons and holes travelling in the direction of an induced electric field are defined not by the drift velocity but by the fermi velocity (c/300). Graphene’s high carrier mobility is directly dependent on the fermi velocity Ref. [5, 10]. The use of the fermi velocity to define the charge carrier speed is due to the zero band gap between the conduction and valence bands. As Fig. 14 shows, the zero band gap meets at a point of two cones, known as a Dirac Cone, which allows electrons to behave like mass-less fermions Ref. [5]. Typical conductors have a gap between parabolic shaped regions. The size of the gap defines the amount of energy required for electrons to leap from the valence
band to the conduction band. Mass-less fermions travel at the fermi velocity \(10^6 \text{ m/s}\) Ref. [5, 10], which is a fraction of the speed of light.

As mentioned early, RF graphene transistors are in use due to graphene’s high carrier mobility, 100 GHz transistors have been achieved with a gate length of 240 nm Ref. [19]. Adopting graphene as the Hall material in MGRAM cell design will give it great potential for improvement of its circuit characteristics (i.e. speed, latency).

Graphene’s electron and hole carrier mobility is limited by the purity of the sample. Intrinsic graphene has zero impurities (no containments during processing) and a perfect honey-comb lattice in all directions (isotropic). Graphene in this form allows for the charge carriers to behave like mass-less fermions but non-isotropic regions will hamper this effect. For example, epitaxial growth of graphene will have isolated regions that are isotropic but overall the entire material would be considered anisotropic. This is due to the boundaries created by isotropic regions. Fig. 11 demonstrates how different growth regions meet and create these boundaries.
If the isotropic regions within a graphene sample are sufficiently large then the boundaries do not occur frequently throughout the sample. Also if the application feature size is within these boundaries then the graphene can practically be classified as isotropic. Another aspect to consider is the material that the graphene is resting upon. The resting material can alter graphene’s carrier mobility.

Graphene layered on silicon dioxide and the silicon (Fig. 12) acts as a capacitor (two plates separated by an insulator). The charge density of the graphene can then be controlled by setting the voltage of the silicon layer.
Another type of structure is suspended graphene, which does not lay on another material (Fig. 13). The suspended graphene exhibits improved electrical properties, such as a carrier mobility of 200,000 cm$^2$/Vs Ref. [6]. Another advancement is to grow graphene on top of a material that has a similar structure, such as hexagonal boron nitride (also a two-dimensional material). Such a structure allows isolating intrinsic graphene due to the substrates’ two-dimensional flatness, leading to an improved manufacturing process Ref. [7].

Graphene grown through chemical vapor deposition (CVD) onto a copper sheet is a conventional method and the obtained carrier mobility is well known. Hence it will be
used as the basis for the rest of the analysis in this paper. Graphene fabricated through CVD can yield a carrier mobility of 5,000 cm$^2$/Vs or greater Ref. [4]. New techniques demonstrate that the smoothness of the copper can be much rougher than the conventional techniques at high temperature, but the CVD method requires that the copper be quite smooth, below 0.6 nm roughness Ref. [8].

![Graphene Dirac Cone](image)

**Figure 14: Graphene Dirac Cone (Zero Band Gap) Ref. [1]**

3.2 Short Channel Effect

The short channel effect will occur in devices with a length less than 100nm. The short channel effect will not be considered in our MGRAM devices design since all devices in this project have a channel length at a minimum of 300nm.

3.3 Back-Gate Voltage Control

A sample of graphene, as noted earlier in Section 3.1, can be back-gate controlled by layering it on top of a dielectric, i.e., silicon dioxide, silicon Caribe, with a silicon layer
underneath it to form a capacitor. Varying the voltage of the silicon will induce a charge
difference in the graphene sample and thus the graphene can be fine-tuned controlled to
have different charge carrier densities. As a result, a sample of graphene with an uncertain
Dirac point voltage (CNP, charge neutrality point) can be optimized to maximize the Hall
sensitivity to an induced magnetic field. Such control eases the fabrication constraints of
the graphene CNP as the device can be calibrated post fabrication for maximum Hall
voltage output. As long as the bulk of the graphene is fabricated similarly (doping effects
are uniform) the CNP will be uniform. In this case the maximum Hall sensitivity can be
calibrated by tuning the back-gate voltage. Leading to the possibility of higher yield per
wafer in part to the ability to fine tune the devices with the back gate voltage.

3.4 Dual Charge-Carrier Graphene Hall Effect

In this section, the dual charge-carrier scenario of graphene and how it enhances
the Hall effect are introduced. Afterward the effect of graphene’s carrier mobility on the
Hall sensitivity is discussed.

Due to graphene’s unique structure (i.e. a linear energy dispersion), the dual
presence of electrons and hole charge carriers is possible. Both carriers are present when
the fermi energy is near the Dirac point (also known as the charge neutrality point, CNP).
The dual charge-carriers scenario increases the Hall coefficient Ref. [1]. An increased Hall
coefficient makes graphene well suited as a Hall sensor material. The important factor is
having both carriers present near the Dirac point. As the fundamental Hall voltage formula
(Eq. 1) has an inverse relationship to the charge carrier density. A smaller charge carrier
density is achieved with graphene compared to traditional Hall materials. Traditional Hall
materials, which have band gaps, stop conducting current at lower fermi energy. The Hall sensitivity increases with decreasing charge density, which occurs at lower fermi energy levels. Low fermi energy levels and low charge carrier density is possible with graphene, leading to greater Hall sensitivity.

Near the Dirac point of graphene, there are two types of charge carriers, electrons and holes. In modeling, unlike the classical Hall material, it requires using non-traditional Hall effect equations: the Fermi-Dirac probability distribution of electrons (Eq. 7, Ref. [1]), the electron density for the regular graphene Hall effect (Eq. 8, Ref. [1]), the electron density for the integer quantum Hall effect (Eq. 9, Ref. [3]), the graphene Hall coefficient (Eq. 10, Ref. [1]), and the graphene Hall voltage (Eq. 11) Ref. [1, 3].

\[
f_{FD, n}(E) = \left( \exp\left( \frac{E - E_f}{k_B T} \right) + 1 \right)^{-1}
\]

\[
n(T) = \int_0^\infty f_{FD, n}(E) \rho(E) dE
\]

\[
N = \Gamma \left[ 4 \sum_{\kappa=1}^\infty \mathcal{F} \left( \frac{\xi \kappa - 1}{\xi} \right) + 2 \mathcal{F} \left( \frac{-1}{\xi} \right) \right], \xi = \frac{k_B T}{E}
\]

\[
R_H = \frac{(n - p)(1 + (\mu B)^2)}{e[(p + n)^2 + (\mu B)^2(p - n)^2]}
\]

\[
V_H = R_H I B
\]

*Equation Variables: \( E_f \) – Fermi Energy, \( \varepsilon_N \) – Normalized Fermi Energy, \( k_B \) – Boltzmann Constant, \( T \) – Temperature, \( n \) – Electron Density, \( p \) – Hole Density, \( B \) – Magnetic Field, \( \mu \) – Carrier Mobility, \( I \) – Current, \( R_H \) – Hall Coefficient, \( e \) – Elementary Charge*
The Fermi-Dirac electron distribution describes the probability of electrons occurring near graphene’s Dirac point. When the Fermi energy, $E_f$ in Eq. 7, approaches the CNP (Dirac point), the distribution of electrons to holes approaches 1:1. Both carriers are present near the CNP. The electron distribution is also dependent on the temperature ($T$) and the Boltzmann constant ($k_B$). The two-dimensional density of states, $\rho(E)$ in Eq. 8, along with Eq. 7 gives the electron density of graphene at a given Fermi energy. The Fermi energy can be controlled directly by the back-gate voltage. The electron density (Eq. 9) is calculated differently for the integer quantum Hall effect and will be discussed later. The Hall coefficient (Eq. 10) is dependent on the magnetic field ($B$), carrier mobility, electron density ($n$), and hole density ($p$), where $n$ and $p$ are dependent on the gate voltage. Shown in Fig. 15 is the graphene Hall coefficient modeled in MATLAB® based upon equations 7, 8, and 10.

![Graphene Hall Coefficient](image)

**Figure 15: Hall Voltage Sensitivity vs. Biasing Gate Voltage**
The Hall Coefficient (sensitivity or gain) vs. gate voltage, demonstrates that the peak sensitivity (maximum Hall voltage) occurs near the Dirac point voltage (Fig. 15). As the Dirac point moves away from the origin, the curve is stretched, and the peak value reduces.

Fig. 16 shows the integer quantum Hall effect (IQHE), which becomes evident at lower temperature and higher magnetic field (Fig. 16 is based upon Eq. 9). Eq. 9 uses the Fermi-Dirac distribution equation at very low temperatures. Clearly visible are the Landau levels (LL) at varying filling factor (Fig. 16 shows the filling factor as $v^{-1}, v^{-1} \sim B$). When magnetic field increases, eventually a new LL is reached. Landau levels are the quantization values of graphene Hall resistivity, as the magnetic field increases and/or the temperature decreases, the LL become more prominent. The IQHE can be detected at higher magnetic fields ($B>20T$, Ref. [10]) or low temperatures ($T<<0^\circ C$). There is a potential that room temperature IQHE at relatively low magnetic field could occur with refinement of graphene. As noted by Novoselov, Ref. [10], the IQHE could be possible in low magnetic fields with improvement of sample homogeneity and charge carrier mobility. The IQHE would enable greater power efficiency in MGRAM, as an equivalent Hall voltage would be attained at a lower read current.
In fabrication, graphene can be transferred after CVD (chemical vapor deposition) onto copper. Graphene electron and hole carrier mobility, from CVD onto copper, can be limited from very high values in the material, such as 100,000 cm$^2$/Vs to around 2,000-5,000 cm$^2$/Vs. The method is cost efficient as it does not use high temperatures, however the defect density is increased due to the structure of the copper that graphene is grown upon Ref. [4, 26]. White impurities present on the copper sheet cause discontinues in the graphene. The copper impurities will also cause growth of multi-layer graphene and not mono-layer graphene Ref. [25]. While lowering the mobility reduces the peak potential gain of the Hall cross, the range of carrier mobility of concern does not greatly affect the gain. The zero band gap is the most important graphene feature which enables it to be a superb Hall material. The zero band gap aspect of graphene allows dual charge carriers to
be present near the Dirac point (or CNP) and increases the maximum sensitivity/gain in the Hall coefficient, which in turn results in higher Hall voltage generation. It is beneficial that the carrier mobility is not the sole factor for performance considering the present processing techniques of graphene. Fig. 17 and 18 show the effect of different charge carrier mobility on the value of Hall resistance at different gate voltages. The gate voltage is a plane voltage separated from the graphene layer by a typical insulator (SiO₂), inducing coupling charge into the graphene. As can be seen in Fig. 17, there is a decrease of peak resistance/sensitivity with decreasing carrier mobility, but even at a low carrier mobility, the gain has not reduced significantly. Typical Hall materials (Si) integrated with CMOS technology have a Hall coefficient of 100. Whereas compared to relatively poor quality graphene with a carrier mobility of 1,000 cm²/Vs has a Hall coefficient of 2000.

![Graphene Hall Sensitivity, Series Varying Carrier Mobility](image)

**Figure 17: Graphene Hall Sensitivity, Series Varying Carrier Mobility**
As shown in Fig. 18 a carrier mobility of 100,000 cm$^2$/Vs yields a peak Hall sensitivity/gain of 2,200. But a drop from 10,000 cm$^2$/Vs to 5,000 cm$^2$/Vs, or 5,000 cm$^2$/Vs to 1,000 cm$^2$/Vs changes the Hall coefficient max performance from 2150 to 2143, or 2143 to 2140, respectively.
CHAPTER 4: MGRAM CHARACTERIZATION & VERILOG-A

METHODOLOGY

4.1 Electrical Circuit Model and Characterization

The purpose of the methodology chapter is to clearly state the characterization process of the MGRAM cell. First a simulation program is used to determine the optimal shape and features of the MGRAM coil and contacts. Following that will be an explanation of the characterization method of the MGRAM core bit write access time. Next the MGRAM read operation characterization is discussed. Lastly the strategy of writing the Verilog-A code is described on how to achieve simplicity and parallel calculations required for a functional product. The analytical model is considered a functional product for its application in a larger integrated circuit design. The following chapter will present and discuss the results.

4.2 MagOasis Magsimus Deluxe

In this study, the simulation program MagOasis Magsimus Deluxe (MMD) is used to characterize the MGRAM coil and ferromagnetic core features and magnetic effects. An optimal coil structure is also researched through the MMD tool. This section details the MMD program in regard to its operation and simulation process.

The MagOasis Magsimus Deluxe simulation program uses finite element numerical analysis to compute small-scale magnetic and electrical field effects. MMD, given a design input, finds the equilibrium magnetic state of the system using solution techniques based on micro-magnetic theory. MMD maintains that the micro-magnetic theory still holds true with pseudo-soft magnets. While the entire system’s free energy
consists of Zeeman energy, exchange energy, magnetic anisotropy energy, and magnetostatic interaction energy, each energy will have an associated effective field.

MMD program simulates the graphene Hall effect based on a dual charge carrier system near the Dirac point (Ref. [1]) and allows configuration of charge density, back-gate voltage, Dirac point voltage, and carrier mobility. The ferromagnetic relationships are considered within each element/cell defined. Each defined structure has multiple adjustable variables such as magnetic permeability, magnetic anisotropy, and exchange coupling. The size and grid of the elements are user defined; changing the number of elements within a system component (such as a coil or a core) can alter simulation system results (i.e. magnetic coercivity) and simulation run time. As each element has its own electrostatic field calculation, increasing the number of elements increases the calculation time and operation complexity.

The exchange coupling variable that affects bulk magnetic permeability, can be adjusted to simulate the hysteresis curve of soft and hard ferromagnetic materials. Simulations can be run using different methods, i.e. Static, Quasi-static, or Dynamic methods, or thermal models (Classical or Stochastic). MMD is an appropriate tool for this research as its effectiveness as a micro-magnetic simulator has been validated [18]. In this study, the MMD program is used to characterize different features of the MGRAM cell.

4.3 Coil Contact Structure

In this section, the characterization method of the MGRAM coil is presented, specifically on the coil’s width, height, and its contact pad orientation. The optimal coil structure was considered in regard to optimizing the output magnet field strength. The
optimal structure was found by changing the width of the coil, the height of the coil, and the coil contact pad size & orientation. The magnetic field strength was described using the Biot-Savart equation (Eq. 12). The contact position and size will be explored for configuration optimizations. Once the optimal structure was identified, it was used as part of the full design simulation.

The Biot-Savart equation gives the basic relationship of a current carrying coil Ref. [27]:

\[ B(r) = \frac{\mu_0 \mu_r I}{4\pi} \int \frac{dl \times a_R}{R^2} \]  

(12)

Figure 19: Magnetic Field from Current-Carrying Coil

The induced magnetic field is larger with a smaller coil radius (r) and/or a longer coil length (l); the magnetic field (B) magnitude is also directly proportional to the current (I). The magnetic permeability of free space (\( \mu_0 \)) and the relative magnetic permeability
(\(\mu_r\)) give the total magnetic permeability of the medium. For Non-magnetic materials, their relative permeability values are close to unity, while for ferromagnetic materials, their relative permeability values are at the order of thousands.

In the MGRAM design, the coil performs the writing of the bit to the ferromagnetic core. When considering the MGRAM cell (Fig. 3), the maximum magnetic flux through the ferromagnetic core was obtained by optimizing the coil dimensions. Optimization leads to the minimal current necessary to reach the magnetization coercivity point. The coercivity point is the point when the ferromagnetic core will flip polarity (see section 4.4). Several simulations were run in MMD tool to characterize the effects of coil feature size and the coil’s contact pads on the induced magnetic field.

*Full* contact pads cover the entire coil contact surface:

![Figure 20: MagOasis Simulation of Coil with Full Contact Pads](image)

Fig. 20 shows a MagOasis simulation setup of just the MGRAM coil with a coil of 100nm width, 250nm height, and a magnetic sensor (in red). The simulation is repeated
multiple times altering the coil width, coil height, and current amplitude. The systematic varying of these parameters characterizes the coil structure and contacts.

*Half* contact pads covers half the coil contact surface:

![Image of MagOasis Simulation of Coil with Half Contact Pads](image1)

*Small* contact pads cover a tenth of the coil contact surface:

![Image of MagOasis Simulation of Coil with Small Contact Pads](image2)

*Figure 21: MagOasis Simulation of Coil with Half Contact Pads*

*Figure 22: MagOasis Simulation of Coil with Small Contact Pads*
The MMD program is developed with a finite element software engine. In the simulation, the coil was defined as a copper-like resistive material, where the coil had 10 layers with each layer containing 25 by 30 array of finite elements.

The effects of using different contact pad orientation and size were studied; Fig. 20-22 show three different simulation setups that were run under the same conditions: 5mA input current, coil height 250nm, coil width 100nm. Only the size and location of the contact pads were changed.

*Full* contact pads with a coil height of 280nm and coil width of 200nm:

![Image](image_url)

**Figure 23: MagOasis Simulation of Large Coil with Large Contact Pads**

The effects of varying the coil width and height were studied; Fig. 23 shows a coil with increased width and height sizes for which several iterations are proposed to find the results of changing these dimensions (height: 180nm, 220nm, 250nm, 280nm; width: 100nm, 200nm). Section 5.2 contains the results of varying the coil size and the contact pads.
4.4 Magnetic Graphene Memory Cell Write Operation

In this section, the MGRAM write operation is described in regard to the ferromagnetic core and how its polarity is switched, and how the hysteresis loop of a ferromagnetic material is induced.

The magnetic graphene memory cell write operation is to store a bit value into the ferromagnetic core. The ferromagnetic core holds this information through a polarized state with its magnetic field pointing up or down (binary state, ‘0’ or ‘1’). The setting of the ferromagnetic core relies on a current carrying coil that induces a magnetic field onto the core/bit. The material is a permalloy (nickel-iron) which typically has a high bulk relative magnetic permeability. As is well known, a ferromagnetic material does not have a constant magnetic permeability but a relative permeability that changes with the external H field, \( B = uH \). Such a feature can be plotted with the hysteresis loop. Simulations carried out in MMD give the important bit-core characteristics.

![Hysteresis Curve of a Ferromagnetic Material](image)

Figure 24: Hysteresis Curve of a Ferromagnetic Material
Fig. 24 shows the coercivity (magnetic field - H field required to reverse the internal field from saturation to zero), the remanence (internal field magnitude after the external field is removed), and the magnetization saturation. The magnetic saturation level is the point when all magnetic domain dipoles are aligned in parallel with the applied H field. The coercivity is the force required to flip the direction of the overall magnetic field of the medium. The remanence is the magnetic field value after the H field is removed.

The simulation efforts were carried out in MMD simulator and subsequent modeling was developed in Verilog-A code. A key aspect studied is the time interval of switching the magnetic core polarity (i.e. write cycle time). To properly characterize the effect, in the modeling, the coil was divided into 30 layers to form a three-dimensional cell array structure. The amount of necessary finite element layers in MagOasis was determined using the trial and error approach. Note, increasing the number of elements until the minute adjustment in results did not merit the increase in simulation run time.

4.5 Magnetic Graphene Memory Cell Read Operation

In this section, the MGRAM device read operation of the ferromagnetic core polarity (i.e. bit value) is detailed. The MGRAM cell read operation was performed by using the graphene Hall cross and the Hall effect. A current was pulsed through one arm of the cross and the Hall voltage sensed through the perpendicular arms (Fig. 25). The Hall voltage was produced since the ferromagnetic core induces a transverse magnetic field on the graphene Hall cross. Depending on the polarity of the ferromagnetic core (‘0’ or ‘1’) the Hall voltage has a different value that can be differentiated.
Before a read operation, the ferromagnetic core is in a steady state where the applied H field from coil is non-existent and the magnetic field of the core maintains its remnant state. The direction of its magnetic field can be read using the graphene Hall cross sensor (the core is one bit of memory). The graphene Hall cross was centered directly underneath the ferromagnetic core (Fig. 4). Insuring the maximum magnetic flux was observed by the graphene Hall sensor. Pulsing a step current through the graphene cross, a Hall voltage is detectable whose value is dependent on the state of the ferromagnetic field. For a hypothetical ‘1’ bit, the magnetic field points down through the graphene Hall cross. As current flows from west to east (see Fig. 25), a positive Hall voltage is sensed on the north arm in relation to the south arm (given a positive Hall coefficient). For a hypothetical ‘0’ bit the magnetic field points up through the graphene hall cross. As current flows west to east (see Fig. 25) a positive Hall voltage was sensed on the south arm in relation to the north arm (given a positive Hall coefficient).
4.6 Model Development of the MGRAM Cell in Verilog-A

The following section will describe the MGRAM model development strategy in Verilog-A code.

The Verilog-A model of the MGRAM cell must accurately and effectively perform read and write operation of the MGRAM cell. The read operation (Hall voltage output) requires the calculation of the graphene Hall coefficient, the ferromagnetic core polarity direction, and the magnitude of the read current. The write operation requires the monitoring of the duration and magnitude of the write current. Also, the model needs to know the current direction of the ferromagnetic core polarity. The resulting integrated circuit model needs to include output voltage nodes for the Hall voltage and an input voltage node for the gate voltage of the graphene. It also needs to have current inputs to the coil and the graphene cross arms for read and write operations. Fig. 26 shows the voltage and current inputs/outputs of the proposed MGRAM Cell Verilog-A symbol. Each of the inputs (write current, read current, and gate voltage) has to be measured and used to calculate the output (Hall voltage), as well as to determine the state of the ferromagnetic core.
Figure 27 shows the necessary Verilog-A code flow. The device parameters in the model development include the width & length of graphene Hall cross, graphene carrier mobility, temperature, write current magnitude and required time duration.
In addition, other physical constants must be saved in the model, such as elementary charge, Boltzmann constant, Dirac voltage, and Planck constant.

The next two stages of the Verilog-A modeling occur in parallel; the Magnetic State Monitor block and the Generate Dual Charge Carrier Array block. The former characterizes the state of the ferromagnetic core and the write current to flip the bit polarity. The latter generates an array of charge carrier density given the device parameters over a range of gate voltage. The selected value from the charge carrier density array determines the Hall coefficient, a key parameter for the MGRAM read operation. The last code block, Calculate Hall Voltage Output, uses all the prior calculations and constant device parameters to calculate the Hall voltage (Fig. 26 V1_HALL & V2_HALL)
Lastly the Verilog-A analytic model performance relies on the simplification of the calculations, ensuring that it is applicable in a larger circuit design simulation. But at the same time simplification cannot compromise the model accuracy.
CHAPTER 5: MGRAM CHARACTERIZATION & VERILOG-A RESULTS

5.1 Electrical Circuit Model and Characterization

The chapter will go over the results based upon the methodology outlaid in the previous chapter. First, simulation results of the optimal shape and features of the MGRAM coil and contacts are discussed. Following that will be a review of the MGRAM core bit write access time. Lastly the Verilog-A code analytical model results will be shown in Figure 36 in comparison to the published graphene Hall cross data, as well as the full MGRAM simulation results.

5.2 Coil Contact Structure Simulation Results

In this section, the characterization results of the MGRAM coil are presented, specifically on the coil’s width, height, and its contact pad orientation. The optimal coil structure is considered in regard to optimizing the output magnet field strength. The magnetic field strength is described using the Biot-Savart equation (Eq. 12). The coil contacts and coil size are shown to have a significant effect on how much magnetic force can be applied to the ferromagnetic core, given a constant current.

The induced magnetic field is larger with a smaller coil radius (r) and/or longer coil length (l); the magnetic field (B) magnitude is also directly proportional to the current (I). The magnetic permeability of free space (μ₀) and the relative magnetic permeability (μᵣ) give the total magnetic permeability of the medium. If no medium is present (i.e. a vacuum) then the permeability equals μ₀ (4π×10⁻⁷). For non-magnetic materials, their relative permeability values are close to unity. Ferromagnetic materials have very high relative permeability values, usually at the order of thousands.
In the MGRAM design, the coil performs the writing of the bit to the ferromagnetic core. When considering the MGRAM cell (Fig. 3), the maximum magnetic flux through the ferromagnetic core is obtained by optimizing the coil dimensions. Table 1 lists the results for all simulation iterations of varying contact type (full, half, & small), coil width (100nm & 200nm), coil height (180nm, 220nm, 250nm, & 280nm), and current (1mA & 5mA).

As the contact pads are separated vertically, the current path takes the shape of a spiral. The greater the contacts are separated with regards to the top and bottom of the coil, the stronger the output of the magnetic field is generated from the coil. Referencing Table 1, the greatest magnetic field output is observed for a 100nm width coil with a height of 180nm and using the Small contact pads. Referring to the Biot-Savart equation, the separation of the contacts increases the effective length of the coil. Contacts at the same height create a current path through one axial plane and the shortest possible path around the coil. By separating the contacts (Fig. 22) the current path took a longer path around the coil. Because the current path length was longer, the effective length of the coil increased. As a result, a stronger magnetic field was produced and observed during simulations. In addition, increasing the current has a linear impact on the magnetic field output as predicted by the Biot-Savart equation (Fig. 28).
Figure 28: Coil Current vs. Magnetic Field Output

Table 1: MagOasis Simulation Results Varying Contact Pads and Coil Dimensions

<table>
<thead>
<tr>
<th>Contact Pad</th>
<th>Input current (mA)</th>
<th>Magnetic Field (Oe)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>180/100 220/100 250/100 280/100 180/200 220/200 250/200 280/200</td>
<td></td>
</tr>
<tr>
<td>Full</td>
<td>11.7 10.9 10.1 9.4 12.2 10.7 10 9.4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>58.4 54.6 50.5 46.9 60.9 53.3 49.9 46.8</td>
<td></td>
</tr>
<tr>
<td>Half</td>
<td>12.9 11.4 10.5 11.1 12.6 11.3 10.5 9.8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>65.6 57.2 52.6 48.7 64.6 56.6 52.6 49</td>
<td></td>
</tr>
<tr>
<td>Small</td>
<td>15.7 13.5 12.2 11.1 15.8 13.8 12.6 11.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>78.7 67.6 60.9 55.4 79.1 69.2 63 57.7</td>
<td></td>
</tr>
</tbody>
</table>

5.3 Magnetic Graphene Memory Cell Write Operation Results

In this section, the MGRAM write operation simulation results are discussed in regard to the ferromagnetic core and its polarity switching. Lastly, the simulated write cycle time is presented.
As mentioned previously, the magnetic graphene memory cell write operation is to store a bit value into the ferromagnetic core. The ferromagnetic core holds this information through a polarized state with its magnetic field pointing up or down (binary state, ‘0’ or ‘1’). The setting of the ferromagnetic core relies on a current carrying coil that induces a magnetic field onto the core/bit. Simulations carried out in MMD characterized the important bit-core characteristics.

The simulation efforts were carried out in MMD simulator and subsequent modeling was developed in Verilog-A code. A key aspect studied was the time interval of switching the magnetic core polarity (i.e. write cycle time). Fig. 29 depicts a 9 ns write access time that was achieved using the optimum coil size (100nm width & 180nm height) as well as the current injection scheme using small contact points (Table 1). These separate injection points allow for the current to spiral.

![Figure 29: Ferromagnetic Core Switching](image)

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The write access time was determined by the amount of time to achieve reversing the bit polarity. As shown in Fig. 29, when the ferromagnetic core goes from the negative magnetic saturation level to the positive magnetic saturation level, it indicated the completion of reversing the bit polarity.

5.4 Memory Storage Medium: Ferromagnetic Core

In this section, the ferromagnetic nickel-iron core is described further in relation to different types (‘hard’ or ‘soft’) of hysteresis shape. Specifics regarding the hysteresis and how it leads to the MGRAM being a non-volatile memory device are discussed.

The ferromagnetic nickel-iron core is a permalloy. The permalloy has a very high magnetic permeability, which is an important characteristic for setting the overall state of a ferromagnetic material. The orientation, domain strain and the shape of the core (radius and height) all play important roles in determining the hysteresis loop in the magnetic core design. The hysteresis loop is the defining characteristic of the core bit. A ‘hard’ magnet has a rectangular shaped hysteresis loop which leads to a larger remnant magnetic field value. A material with an elliptic shaped hysteresis loop is typically consider a ‘soft’ magnet, which has a smaller remnant value. Important points to consider on the hysteresis loop are the magnetic saturation, coercivity, and remnant values. The hysteresis loop is a representation of the relationship between the applied H field and the resulting M field.

The following describes the H & M field relationship in a ferromagnetic, referencing Fig. 24 start at the origin. As the external H field increases in strength, the magnetization of the ferromagnet increases correspondingly in a parallel direction. Then the magnetic domain dipoles within in the ferromagnet start to align in one direction.
all domains are aligned, the magnet is saturated. When H field decreases and vanishes, the magnetically aligned ferromagnet stabilizes in its remnant state.

The shape of the magnetic domains dictates their tendency to point in a certain direction (anisotropic versus isotropic material). Anisotropy magnetic materials tend to be ‘soft’ magnets: when the H field is removed, several domains relax back to their preferred direction. Thus the overall magnetic state will decrease to its remanence. Remnant and magnetic saturation values approximately close to each other denotes a ‘hard’ magnet. Such a material will have a high magnetic permeability and sustains the direction of the absent H field. The ability to sustain polarity and store information is the reason that nickel-iron ferromagnets are used in other storage mediums such as hard-disk drives. Even after the H field is removed, the value stored (magnetic direction) persists. The ability of the MGRAM ferromagnetic core to sustain its polarity makes it non-volatile.

5.5 MGRAM Cell in MMD & Verilog-A Results

The following section describes the MGRAM model development in Verilog-A code, presents device read/write results and the full design simulation results in MMD.

The Verilog-A model of the MGRAM cell was developed upon the behavior of graphene and ferromagnetic materials, as well as considering the fundamental read and write operation of the MGRAM cell. Verification of the Verilog-A code was performed by examining the Hall coefficient outputs of the circuit schematic and the characteristic formulas.

The Fermi-Dirac distribution and electron/hole density (Eq. 7, 8) are at the core of the model whose solution is rendered numerically by summation of the area as opposed
to an analytical solution. The Fermi-Dirac distribution is shown in Fig. 30, with the area in orange being the probability that electrons are present and the area in blue being the probability that holes are present. In the example shown in Fig. 30 the probability for holes or electrons to be present is equivalent because the Fermi energy is at the Dirac point. The calculation was used in the code *Generate Dual Charge Carrier Array* block (see Fig. 27).

![Fermi-Dirac Distribution](image)

**Figure 30: Fermi-Dirac Distribution Ref. [1]**

The Verilog-A model calculates the area under the Fermi-Dirac curve to determine the probability of electrons and holes. Calculating the area in Verilog-A code is simpler than attempting to write an integrator to solve Eq. 8 analytically. Fig. 31 shows the output from Eq. 8 based on the Fermi energy. As the energy level moves away from the Dirac point, the probability of both charge carriers being present decreases. The result is the density of one carrier soon dominates the other.
Eq. 7 is the basis for calculating charge carrier density and hence the graphene Hall coefficient. Calculating it precisely, especially near the Dirac point, is paramount to obtaining an accurate model.

**Figure 31: Electron & Hole Density vs Fermi Energy**

Transferring Eq. 7 into Verilog-A code requires breaking out the array arithmetic, in the *Generate Dual Charge Carrier Array* code block:

```verilog
for (m=1; m<=321 ; m=m+1)
begin
    for (j=1; j<=1201; j=j+1)
    begin
        DOCn[j] = abs(Eplus[j]+Ef_shift)/(exp((Eplus[j]-Ef[m]+Ef_shift)/kB_T)+1);
        //DOCn is the Density of electron charge carriers at one fermi energy level
        //Eplus is an array of positive fermi energy values, Ef_shift is the Dirac point voltage in
        //fermi energy units, kB_T is a constant of Boltzmann constant times the given
        //temperature
```
\[ \text{DOCp}[j] = \frac{\text{abs}(\text{Eneg}[j]+\text{Ef}_\text{shift})}{\exp\left(\frac{(\text{Ef}[m]-\text{Eneg}[j]-\text{Ef}_\text{shift})}{k\cdot B\cdot T}\right)+1}; \]

// DOCp is the Density of hole charge carriers at one fermi energy level
// Efplus is an array of negative fermi energy values

\[ \text{DOCn}_\text{sum}=\text{DOCn}_\text{sum}+\text{DOCn}[j]; \]
\[ \text{DOCp}_\text{sum}=\text{DOCp}_\text{sum}+\text{DOCp}[j]; \]

// DOCn_sum and DOCp_sum is the summarization of density across all fermi energy

end
end

The section of Verilog-A code (see Appendix for complete full version) output closely follows the equation set (Eq. 7, 8, 10), which determine the graphene Hall effect characteristics. The summation method used in the model matches the actual calculation using the full integration method, as demonstrated in Fig. 32 where the full integration method was plotted over the model summation method. The complete integration calculation and the model calculation overlay each other closely.

![Graph of R_H vs Gate Voltage](image)

**Figure 32: MATLAB and Verilog-A Simulation Results of the Hall Coefficient**
Fig. 32 plots the applied gate voltage (range -30V to 30V) versus the calculated Hall coefficient. The Dirac point voltage (CNP) was set to 13V, which corresponds to the zero-crossing point of the Hall coefficient.

As discussed earlier, the MMD tool was used to simulate graphene and the ferromagnetic core. Fig. 33 is an example of testing the graphene sample to multiple read/write cycles in MMD.

![Figure 33: Overlayed Read and Write Cycles](image)

Fig. 34 gives the output of testing the MGRAM cell (Fig. 3) through a write cycle for the original coil dimensions and contact pads, and for the optimized coil and contact pads. The optimized coil (small separated contacts, a coil height of 180nm, and a coil width of 100nm) was the better performing design and preferred choice for the MGRAM cell. As shown the optimized coil obtains a higher magnetization level of the ferromagnetic core, facilitating greater Hall voltage difference between a ‘1’ and ‘0’ bit. Less write
current can also be used with the optimized coil to reach a similar magnetization level as the original coil.

![Ferromagnetic Core Magnetization Graph](image)

**Figure 3: MagOasis Simulation Output of Writing Cycle**

The graph in Fig. 34 also shows how the polarity of the ferromagnetic core can be effectively switched. When a current is pulsed through the coil, an H field is generated. The H field produced is in the opposite direction of the ferromagnetic core’s magnetic field. Previous results (Fig. 29) show that when the current is sustained for a 9 ns pulse, it switches the polarity of the core. Fig. 33 demonstrates the overlaying read and write cycles of the MGRAM memory device, where the write access time is 9 ns while the read access time is less than 1 ns. Ultimately the read access time is limited by the sensing circuitry of the Hall voltage.

Finally, Fig. 35 shows the output Hall voltage from a Cadence circuit simulation using the MGRAM cell Verilog-A model. It shows how pulsing a writing current (step wave) changed the polarity of the ferromagnetic core and changed the magnitude of the
Hall voltage. The Hall voltage difference (between the north and south arms of the graphene Hall cross) obtained is 100 mV where a constant read current of 50 uA was applied. The switching aspect is also shown, based on prior simulations, to be under 10ns.

![Figure 35: Verilog-A MGRAM Cell Simulation Result of Write Cycle with Constant Read Current](image)

Lastly, the output of the Verilog-A model Hall voltage is compared to published experimental data of a graphene Hall cross in Fig. 36. The chart shows the linear relationship between Hall voltage and induced magnetic field in the range of -2 T to 2 T. The test configuration is included in the chart (50 uA read current, 5.5 V gate voltage, 13 V Dirac point voltage). The blue line is obtained from the published graphene Hall paper, Ref. [2], and the green line is the output from the Verilog-A model.
Figure 36: Verilog-A Model Compared to Graphene Hall Cross Published Experiment Data

Given that CMOS voltage sense circuitry is required, it must be included in the read access time, 5-12 ns for 65 nm CMOS Ref. [26]. But once sensing technology improves, with either new materials or enhanced designs, the MGRAM device will be able to tap in its potential read speed.
CHAPTER 6: CONCLUSION

Memory design plays an important role in modern computer technology in regard to overall performance and reliability. Memory technologies such as DRAM, SRAM, and ROM have limitations in regard to volatility and robustness that can hamper current IC designs. The MGRAM cell memory device addresses these limitations since it utilizes the reliability of magnetic memory (non-volatile) and superior electrical properties of graphene (high carrier mobility, zero-band gap, high Hall sensitivity).

In this research, a graphene Hall effect model was created to facilitate for the MGRAM cell circuit design and simulation. Several performance affecting aspects were considered, including temperature, graphene carrier mobility, coil optimal dimensions, contact pad optimal dimensions, sufficient write current, etc. The background prior art search also verified that graphene is indeed a better choice for a Hall effect material compared to industry standards (silicon CMOS sensors). Finally, all these considerations were taken into account in the Verilog-A model.

The Verilog-A model results show a maximum Hall effect voltage of 100mV for a bias current of 50uA with a 1 Tesla magnetic field, a writing cycle of 9 ns for setting the magnetic state, and a reading cycle even less than 5-12 ns due to the electrons in graphene travelling at the fermi velocity (c/300). The Verilog-A model developed continuously measures the read current, the write current, and the gate voltage. With the applied gate voltage, the model accurately calculates the graphene electron density, hole density, and output Hall voltage. It also measures the duration of the write current. When the current is sustained for a duration of 9ns, the bit value of the cell is set. The model also considers the magnetoresistance effect induced by the ferromagnetic core magnetic field, and
characterizes the changes of the voltage conditions on the nodes of the read cross arm (see Fig. 5 & 25). The voltage node calculation is based on the bias current and induced magnetic field from the ferromagnetic core.

Graphene magnetic memory technology is in its infancy and the potentials for improvements are very likely in the near future such as using the IQHE (Integer Quantum Hall Effect). Once graphene IQHE is achieved at room temperature and low magnetic fields, the MGRAM memory cell could bridge the gap to quantum devices being integrated into present day technologies. Future research into the fabrication of graphene will be key for the material being usable in commercial applications (i.e. advancements in cheaper production). Also, graphene’s promising electrical properties will not reach their full potential unless further work is done to discover improved processes that produce intrinsic graphene without containments. In addition, other innovations are necessary to discover practical means of integrating graphene with other technologies such as current semiconductors and other new emerging materials.

Going forward, the developed Verilog-A model can be used for future design work as a foundation for developing newer models when graphene and magnetic memories progress. The model is a building block that can be integrated with other emerging technologies and materials in a traditional circuit simulation program.
REFERENCES


APPENDIX

A.1 Verilog-A Code

// VerilogA Hall Effect Model, UVM -- Gregory Abrami -- 1/21/15

`include "constants.vams"
`include "disciplines.vams"

module Hall_Effect_Model_test(in,out,v1,v2,Vg,high,low);

inout in,out,high,low;
electrical in, out, v1, v2, Vg, vh1, vh2, high, low, mid;
parameter real u=0.5, T=293, W = 100, L = 300, thresh=50e-3, ttol = 6e-9;
real DOCn_sum;
real DOCp_sum;
real RH;
real Rxx;
real P;
real R, RL;
real Eplus[1:1201];
real Eneg[1:1201];
real Ef[1:321];
real DOCn[1:1201];
real DOCp[1:1201];
real n[1:321];
real p[1:321];
real VGATE[1:321];
real Vff;
real theta;
real zeta;
real epn;
real ns;
real x;
real t,t0,t1,B;
real Rcoil;

integer m, i, j, y, z, N, armed, armed2;
localparam real alpha=7.154e14, q=1.609e-19,
  h=6.5821e-16, vf=1e6, kB=8.617e-5, Vd = 0, Ef_shift = 0.0;

analog
begin
  @(initial_step)begin


armed=0; armed2=0; Rcoil = 1;
end

V(high,low) <+ Rcoil*I(high,low);

// sense and record the start of the interval
t0 = last_crossing(abs(I(high,low)) - thresh, 1);
@ (cross(abs(I(high,low)) - thresh, 1)) begin
  armed = 1;
  armed2 = 1;
end

// sense and record the end of the interval
t1 = last_crossing(abs(I(high,low)) - thresh, -1);
@ (cross(abs(I(high,low)) - thresh, -1)) begin
  if (armed) begin
    armed = 0;
  end
end

if ($abstime-t0 >= ttol && armed2==1) begin
  //set bit value to either 1 or 0
  if (I(high,low) > 0) begin
    B = 1;
  end
  else begin
    B = -1;
  end
  armed2=0;
end

for (i=1; i<=1201; i=i+1) //Initializing data vectors Eplus,Eneg
begin
  Eplus[i] = 0.0+(0.001*(i-1));
  Eneg[i] = -1.2+(0.001*(i-1));
end

for (i=1; i<=321; i=i+1) //Initializing data vector Ef
begin
  Ef[i] = -0.16+(0.001*(i-1));
end

DOCn_sum=0.0;
DOCp_sum=0.0;
for (m=1; m<=321 ; m=m+1)
begin

for (j=1; j<=1201; j=j+1)
begin

DOCn[j] = 1.4694e18*abs(Eplus[j]+Ef_shift)/(exp((Eplus[j]-Ef[m]+Ef_shift)/(kB*T))+1); //DOCn is the Density of electron charge carriers at one fermi energy level
//Eplus is an array of positive fermi energy values, Ef_shift is the Dirac point voltage in //fermi energy units, kB_T is a constant of Boltzmann constant times the given //Temperature

DOCp[j] = 1.4694e18*(abs(Eneg[j]+Ef_shift))/(exp((Ef[m]-Eneg[j]-Ef_shift)/(kB*T))+1); //DOCp is the Density of hole charge carriers at one fermi energy level ///// Eplus is an array of negative fermi energy values

DOCn_sum=DOCn_sum+DOCn[j];
DOCp_sum=DOCp_sum+DOCp[j]; //DOCn_sum and DOCp_sum is the summarization of density across all fermi energy

end

n[m] = 0.001*DOCn_sum;
p[m] = 0.001*DOCp_sum;
DOCn_sum=0.0;
DOCp_sum=0.0;
end

x = V(Vg); //Read the current gate voltage
j=1;
for (m=1; m<=321 ; m=m+1)
begin

VGATE[m] = Vd + (n[m]-p[m])/alpha;

if (x < VGATE[m] & & j==1)
begin
y=m;
j=0;
end

end

x = V(Vg); //Read the current gate voltage
j=1;
for (m=1; m<=321 ; m=m+1)
begin

VGATE[m] = Vd + (n[m]-p[m])/alpha;

if (x < VGATE[m] & & j==1)
begin
y=m;
j=0;
end

end
//Calculate the Hall Coefficient
RH = (n[y]-p[y]) *(1+(u*u*B*B)) /((q*(p[y]+n[y]))*(p[y]+n[y])+((u*u*B*B)*(p[y]-n[y]))*(p[y]-n[y])));

//Calculate the Magnetoresistance Effect
Rxx = (n[y]+p[y]) *(1+(u*u*B*B))/((q*u*((p[y]+n[y]))*(p[y]+n[y]))+((u*u*B*B)*(p[y]-n[y]))*(p[y]-n[y])));

R = ((L/W)-1)/((n[y]+p[y])*q*u);

V(in,out) <+ (Rxx+R)*I(in,out);

V(mid) <+ V(in) - (0.5*(Rxx+R)*I(in,out));
V(mid,vh1) <+ (RH*I(in,out)*B)/2;
V(vh2,mid) <+ (RH*I(in,out)*B)/2;

V(vh1,v1) <+ I(vh1,v1)*((Rxx*0.5)+R);
V(v2,vh2) <+ I(v2,vh2)*((Rxx*0.5)+R);

end
endmodule