Temperature Dependent Charge Transport Characteristics of Ferroelectric Organic Field Effect Transistors

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Temperature Dependent Charge Transport Characteristics of Ferroelectric Organic Field Effect Transistors

by

Jared C. Benson

A Thesis submitted to the Faculty of the University of Vermont
College of Arts and Sciences in partial fulfillment
of the requirements for the degree of
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Abstract

In recent decades, organic semiconductor materials have emerged as an attractive alternative to inorganic compounds for electronics applications. One application where organic semiconductor materials show particular potential is in the fabrication of transistors, such as organic field-effect transistors. These transistors modulate and switch electrical signals by utilizing a transverse electric field to influence charge transport across the transistor channel. In this project, a top-gate bottom-contact organic field-effect transistor architecture was modified to enable the addition of a ferroelectric polymer as the gate dielectric. These transistors, known as ferroelectric organic field-effect transistors, exhibit a characteristic hysteresis in their transfer properties as a result of the dipolar polarization states present in the ferroelectric polymer, making them excellent candidates for non-volatile memory applications. In this project, functional transistors were fabricated based on the developed experimental methodologies and characterized both in air at room temperature and under vacuum at varying temperatures. These transistors exhibited strong ferroelectric properties, with differences in source-drain current as high as four orders of magnitude between polarized and unpolarized states of the ferroelectric dielectric layer at zero gate bias. Transistor performance was also evaluated through the calculation of linear charge carrier mobility. For the samples measured at room temperature, the highest linear mobility was estimated to be 0.18 cm$^2$/V*s. Measurements taken under vacuum at variable temperatures followed expected trends. The relatively low performance observed in these Fe-OFETs is indicative of imperfections in the fabrication procedure, which still has a significant amount of room for refinement. Temperature dependence data collected from one transistor serves as a baseline for further Fe-OFET temperature dependence experiments. Overall, this project established a foundation on which further studies of ferroelectric transistors at UVM can build.

1Note that this project was cut short when UVM’s labs were closed in March 2020 due to the COVID-19 pandemic. This closure reduced the time that data could be collected by approximately one month. The last month in a project such as this one is often the most productive, so it is possible that the results would have been much more complete had the pandemic not occurred.
Acknowledgments

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Chapter 1: Background

1.1 Transistor Basics

Semiconductor materials form the basis of transistor devices. At a fundamental level, semiconductors are intermediaries between insulating and conducting materials. They exhibit electronic properties that vary based on the physical and electrical conditions they are subjected to. For instance, the conductivity of a semiconductor typically increases with increasing temperature, opposite the behavior that a metal would exhibit. Different types of transistors utilize these properties to control electrical current in various ways. This project focused on field-effect transistors (FETs). In such transistors, electrical current must pass across a channel containing the semiconducting material. In order to influence the behavior of charge carriers, a voltage can be applied to the gate electrode, inducing a transverse electric field in the transistor channel. This electric field serves to modify the effective electrical dimensions of the channel [1]. Depending on the structure of the transistor, this can increase or decrease the rate at which charge carriers pass between the source and drain electrodes. Thus, by altering the voltage at the gate electrode, it is possible to use a field effect transistor to amplify or switch electrical signals.
1.2 Organic Semiconductor Materials

Field effect transistors were initially universally fabricated using inorganic compounds. More recently; however, organic compounds have come to be seen as an attractive alternative. While these organic materials exhibit lower performance when compared to their inorganic counterparts, there are other areas in which they excel. One of the primary benefits of using organic semiconductor materials is the ease with which they can be processed. Inorganic materials often require high-temperature, high-vacuum deposition conditions in addition to advanced photolithographic techniques [1]. Contrary to this, some organic semiconductor materials can be processed using techniques such as solution processing which are more straightforward and cost-effective. In solution processing, the semiconductor material is put into solution with a solvent and processed onto the recipient sample. Once the solvent evaporates, a semiconducting film is left behind. The quality of the resulting film is highly dependent on the conditions under which the solution was processed. Thus, the experimental methods utilized in transistor fabrication are incredibly impactful on the eventual performance of the resulting transistors. Besides ease of processing, organic semiconductor films are much more mechanically flexible than their inorganic counterparts. These properties make organic semiconductor materials prime candidates for applications that require flexible circuits, particularly in situation where low power operation is desirable. Finally, by using chemical processes to change the physical structure of organic semiconductors, it is possible to tailor a material to the specific requirements of its eventual applications. All these factors combine to make the fabrication of organic field effect transistors appealing for many real-world applications, such as flexible displays.

There are a number of theories that explain the charge transport mechanisms present in organic semiconductor materials. One such model finds that the behavior of charge carriers in organic semiconductor materials follows a law that relies heavily on tempera-
ture. At low temperature, the transportation of charge relies on purely quantum effects; however, at larger temperatures, charge transport is said to rely on the tunneling of charge carriers [2]. However, the validity of this model has recently come into question. The hopping model makes the assumption that the intermolecular transfer energy is the smallest present energy scale; however, in organic semiconductor materials, there are several microscopic interactions with comparable energy scales [3]. More recently, a model has suggesting that the charge transport scheme relies instead on transient localization. The transient localization scheme for charge transport is based on the fact that organic solids are generally held together by weak van der Waals forces. Due to the weak forces holding the molecules together, oscillations due to thermal effects within the semiconducting material are slow but can have large amplitudes. These oscillations have significant impacts on the behavior of charge carriers because they create an uneven energy environment within the organic semiconductor material [3]. Dynamic disorder induced irregularities in the energy environment severely hinder the mobility of charge carriers in the material. Transient localization posits a theory that also exhibits a strong temperature dependence, similarly to the hopping/tunneling model above.

1.3 Organic Field-Effect Transistors

When transitioning from inorganic to organic semiconducting materials, fabrication techniques must be altered to account for new materials in not only the semiconductor layer but also the gate dielectric layer. In some cases, an oxide that would typically be used as for this layer in an inorganic field effect transistor is replaced with a polymer that can be solution processed. There are two main organic field-effect transistor (OFET) architectures corresponding to the position of the gate electrode: top-gate and bottom-gate. These two architectures are further delineated into top-contact and bottom-contact
varieties based on the position of the contacts relative to the semiconducting layer. These four total architectures are shown below in Fig. 1.1.

![Organic field-effect transistor architectures](image)

**Figure 1.1:** Organic field-effect transistor architectures.

Each of these architectures has both benefits and drawbacks and is usually selected based on the materials to be used in the experiment.

### 1.4 Ferroelectric Organic Field Effect Transistors

One impactful way the OFET architecture outlined above can be altered is with the use of a ferroelectric polymer for the gate dielectric layer, resulting in a ferroelectric organic field-effect transistor (Fe-OFET). Ferroelectric polymers differ from the usual unipolar gate dielectric layers in that they have dipolar polarization states. This is illustrated by the capacitor curve in Fig. 1.2 provided by Richards Miller, which shows the capacitance vs
voltage for a capacitor made using the ferroelectric copolymer poly(vinylidene fluoride-co-trifluoroethylene) (P(VDF-TrFE)) at 11.1 kHz [4].

As this plot shows, at applied voltage values $V = \pm 20$ V, the P(VDF-TrFE) in the capacitor switches polarization states due to the electric field in the capacitor induced by the applied voltage. This results in the hysteresis visible when comparing the directions of the voltage sweep. Hysteresis in P(VDF-TrFE) is a direct consequence of the properties of poly(vinylidene fluoride) (PVDF), namely the strong dipole moment of the PVDF monomer unit which results from the difference in electronegativity between fluorine atoms compared to the hydrogen and carbon atoms [6]. When PVDF transitions from an unpolarized state...
to a polarized state from the applied voltage, the dipole moment of each polymer chain transitions from a random orientations to the orientation dictated by this voltage. Changing polarization states means that the dipole moments of each polymer chain switch from one orientation to another. Essentially, when the capacitor reaches ±20 V, the dipole moment of the P(VDF-TrFE) layer inverts its polarization, causing the differences in capacitance as the voltage sweeps in the other direction. PVDF has several phases, of which the three most commonly used are shown in Fig. 1.3.

Figure 1.3: α, β, and γ phases of PVDF [6].

Each chain has an individual dipole moment, such that they contribute to the overall dipole moment of the bulk material differently depending on how they are packed. Additionally, electronic properties of PVDF are inherently tied to the phase it is in. The β-phase has the highest dipole moment per unit cell and exhibits the best ferroelectric properties, so this phase was the most desirable for this project. The copolymer P(VDF-TrFE) ensures that PVDF is always in the β-phase due to the presence of the third fluoride in the TrFE monomer unit, which induces the β-phase by favoring all-trans conformation [6]. The structure of P(VDF-TrFE) is shown in Fig. 1.4.
Because of the inclusion of P(VDF-TrFE) in the transistor’s structure, the properties of its dielectric layer are now significantly different as they now depend on the polarization state of the ferroelectric polymer. Since these states can be programmed using the gate electrode, and the current across the channel of the transistor can differ by orders of magnitude depending on which state the transistor is programmed in, Fe-OFETs can serve as non-volatile memory devices. Due to these unique properties, Fe-OFETs have a lot of possible applications in portable electronics where small form-factor, low power, and potentially flexible electronics are needed. These circuits need non-volatile memory, and Fe-OFETs have the potential to serve in this capacity.
1.5 Selected Transistor Structure

Figure 1.5: Selected ferroelectric organic field-effect transistor structure.

Figure 1.5 shows the final transistor structure settled upon in this project. The overall structure was top-gate, bottom-contact. This architecture was chosen due to the desire to minimize the effects of contact resistance in these transistors. The semiconductor material used was 2,7-Dioctyl[1]benzothieno[3,2-b][1]benzothiophene (C8-BTBT), which was selected for its high carrier mobility as well as previous experience working with it. The ferroelectric dielectric material selected was the ferroelectric copolymer P(VDF-TrFE), which was chosen for its strong ferroelectric properties. Other layers and treatments are justified on an experimental basis and are discussed in the next chapter. Figure 1.6 shows how the two polarization states in the transistor facilitate charge transport in different manners depending on whether positive or negative voltage is applied at the gate electrode.
Figure 1.6: Visualization of the differences in charge transport between the two polarization states of P(VDF-TrFE).
2.1 Substrate Preparation

Fused silica (SiO2) substrates in a 20 mm by 15 mm rectangular format were selected for the samples used in this project. Fused silica proved to be fairly durable and easy to work with. The chosen form factor was selected for convenience as well as its compatibility with existing fabrication techniques. Each of these substrates held 20 transistors, which allowed for a reasonable amount of data to be collected from each sample. The fused silica substrates used were fabricated by Valley Design Corp. using Corning 7980 High Purity Fused Silicia (HPFS), a UV grade fused silica wafer material [7]. In addition to its other beneficial properties, this fused silica exhibits low thermal expansion behavior, which lends to its use in a temperature dependence experiment.

Before the transistor fabrication process could begin, the substrates had to be cleaned of any microscopic contaminants present on them. This was accomplished through the use of an ultrasonic cleaner, which utilizes ultrasonic vibrations propagating through a liquid medium in order to clean objects [8]. The substrates were cleaned for 10 minutes each in deionized water, acetone, and isopropanol respectively.
2.2 PTES Treatment

To improve the quality of the films by discouraging the dewetting of the semiconductor solution due to possible remaining contamination, the substrates were then treated with Trichloro(phenethyl)silane (PTES). A 3 mMol solution of PTES in Toluene was prepared in a reaction chamber. The samples were lowered into the solution. The reactor was heated in a 110 °C oil bath and supplied with nitrogen gas. The ensuing reaction was allowed to proceed for 15 hours, after which the samples were removed and rinsed in toluene.

2.3 Thermal Evaporation of Gold

Figure 2.1: Vacuum chamber used in the gold deposition (left) and source-drain shadow mask [9] (right).
The first layer deposited on the cleaned substrates was a thin layer of gold that served as the source and drain contacts for the transistors. Gold was selected for the source and drain contacts because of its favorable electrical properties, particularly its high conductance. The substrates were loaded into an evaporation stack with Ossila high density source-drain shadow masks which was in turn loaded into vacuum chamber. Two filaments were fashioned from tungsten wire, and subsequently wrapped with short segments of gold wire. These filaments were mounted in the chamber, which was pumped down to \(5.0 \mu\text{Torr}\), at which point the gold deposition was carried out. Voltage was applied through the tungsten filaments from external terminals, increasing gradually until the filament reached its maximum current of 20.5 A. At this point the gold evaporated off the filament and through the shadow masks onto the samples. The deposited source and drain contacts’ dimensions were such that the length and width of the transistor channel for all the transistors on each sample were 30 microns and 1000 microns, respectively.

The above specified method for gold deposition was utilized for samples measured at room temperature. Samples to be measured at varying temperatures needed more robust contacts to avoid contact damage preventing the experiment from continuing as many measurements had to be taken of the same transistor. To increase the durability of the source-drain contacts, two-metal contacts were deposited. First, a layer of chromium was deposited, on top of which gold was deposited.
2.4 PFBT Contact Treatment

Once the source and drain contacts were deposited on the substrates, they were treated with 2,3,4,5,6-Pentafluorothiophenol (PFBT). The thiol group in PFBT is attracted to the gold source-drain contacts. Thus, when the samples were submersed in a PFBT solution, PFBT molecules formed a self-assembled monolayer on the source-drain contacts. The PFBT monolayer serves to induce a dipole at the surface of the contacts, which modifies the work function of the contacts, reducing the contact resistance between the gold and the semiconductor layer to be deposited next [10]. This step is important because contact resistance limits charge injection in the channel, which is a significant bottleneck in transistor performance. In order to apply the PFBT treatment, the samples were submersed in a 10 mMol solution of PFBT and Isopropanol. After 15 minutes had elapsed, the samples were removed from this solution, rinsed in toluene, blown dry with air, and for 5 minutes at 60 °C.
2.5 Writing C8-BTBT Films

Figure 2.2: Pen-writing C8-BTBT (left) and polarized photo of sample after C8-BTBT was written (right).

The semiconducting layer was pen-written on each sample using a microslot writer. This writer, shown in Fig. 2.2, consists of a reservoir with four parallel channels all leading to a vertical slot in the writer that extends from the bottom of the microslot writer towards the substrate below. When a liquid is loaded into the microslot writer, adhesive and cohesive forces act on the liquid, resulting in the liquid forming a droplet on the surface of the substrate that moves with the microslot writing head. This droplet leaves behind a film of solvent that evaporates, such that the end result is the desired semiconducting layer.

In order to write a C8-BTBT film, first a 1.5% weight solution of C8-BTBT was prepared. The samples were adhered to motorized linear stage using a small application of vacuum grease on the bottom of each sample. To attain ideal writing conditions, each
sample was heated to and kept at 60 °C while the C8-BTBT film was written. The films were written at a linear speed of 25 mm/s. An image of a sample C8-BTBT film is shown in Fig. 2.2, illustrating the material’s polarization contrast.

2.6 Spin Coating Dielectric Layers

![Figure 2.3: The spin coater used (left) and its control panel (right).](image)

Two dielectric layers were written over top of the C8-BTBT semiconducting layer. Both these layers were written using a Laurell spin coater shown in Fig. 2.3. This technique allowed for finer control over the thickness and consistency of these films compared to the pen-writing process used for the previous step. A spin coater functions by spinning the sample with a high rotational speed. First, the substrate is attached by vacuum to the chuck of the spin coater. Next, the sample is covered in the solution to be written on
the sample. During the spin-coating process, the rotational motion of the sample propels excess solution off of the sample, resulting in a layer of the desired thickness.

The CYTOP layer written directly over top of the C8-BTBT film served two purposes. First, it hoped to serve as a buffer between the semiconducting layer and the ferroelectric layer, given that buffer layers have been shown by to reduce polarization fluctuations in the ferroelectric layer [11]. Reduced polarization fluctuations are desirable given that polarization fluctuations are extremely harmful to device performance as they increase the disorder of charge carriers in the transistor channel. The CYTOP layer also protected C8-BTBT layer from the solvent used with the later P(VDF-TrFE) layer, which would otherwise have damaged the semiconducting layer. Given these objectives, the CYTOP layer was intentionally thin. A 1:1 solution of CYTOP 809M and CTSOLV 180 was used at a high speed of 4000 rpm for 45 seconds. To improve the characteristics of this film, it was annealed for 1.5 hours at 60 °C.

The second dielectric layer was the ferroelectric dielectric layer. To deposit this layer, a 100 mMol solution of Solvene P300, which is composed of 30 mol % trifluoroethylene (TrFE) and 70 mol % vinylidene fluoride (VDF), was first prepared in 2-Butanone. In order to ensure the ferroelectric properties of the transistors were easily visible, a much thicker film of Solvene was deposited. To this end, the Solvene solution was spin coated onto each sample at 1000 rpm for 1 minute. The Solvene films were annealed for 2 hours at 60 °C.

In order to evaluate transistor performance later on, it was necessary to measure the
thickness of both dielectric layers. An additional fused silica substrate was used for this purpose. This sample was coated with both CYTOP and Solvene, and the thickness of the films on the sample was measured with a profilometer. The first thickness measurement determined the thickness of the CYTOP layer (100 nm) and the difference of the first and second measurements determined the thickness of the Solvene layer (1200 nm).

2.7 Thermal Evaporation of Aluminum

The final layer to be deposited on the samples was aluminum, which served as the gate contact for the transistors. This evaporation took place in a bell jar evaporator and based off of similar principles as were present in the gold evaporation. The samples were loaded into an evaporation stack with appropriately shaped cutouts for the gate contacts.
Then, this assembly was loaded into the bell jar evaporator. Unlike before, the filament used was basket shaped, such that the aluminum wire to be evaporated was hung in a ‘shrimp cocktail’ configuration. The bell jar was pumped down to a pressure of 5.0 μTorr. Next, the filament was gradually brought to a voltage of 90 V where it was left for 10 minutes. After the filament was slowly turned off and the bell jar was allowed to cool, the bell jar was depressurized, and the samples were removed. This step concluded the fabrication of the transistors.

2.8 Room Temperature Measurements

The first measurements made in the characterization of the transistors were taken at room temperature. These techniques allow for the determination of key aspects of the functioning and performance of transistors while also retaining efficiency in data collection. To make these measurements, the sample being measured was loaded onto a stage under the probe station. Using a microscope, each of three probes were aligned with their respective contacts on the transistors and then lowered such as to make contact with the contacts on the transistor being measured. This measurement setup is illustrated in Fig. 2.5 below.
For each transistor that was measured, the IV and transfer characteristics were determined. To measure the IV characteristics, the gate voltage was first fixed. The current between the source and drain contacts was measured as the voltage of the drain contact was swept across a range of values. This process was repeated for a number of other gate voltages. The transfer characteristics were measured by first fixing the voltage at the drain contact, and then the source-drain current was measured between the source and drain.
contacts as the gate voltage was swept.

2.9 Temperature Dependent Measurements

Temperature dependent measurements were considerably more involved than the room temperature measurements. Samples to be measured under varying temperatures were loaded into a probe station in a vacuum chamber like the one pictured in Fig. 2.6.

![Vacuum probe station](image)

Figure 2.6: A vacuum probe station like the one used in this project [13].

This chamber was then pumped down to a pressure of 50 μTorr. The temperature of the samples was then regulated using both a heater and a supply of liquid nitrogen from a portable dewer. The sample was cooled from room temperature to 80 K, with measurements made every 20 K. To make these measurements, probes were adjusted to the
correct positions using a camera that looked in a window in the vacuum chamber. Each measurement was otherwise identical to those taken at room temperature as specified above. Several measurements were taken as the sample was raised back to room temperature from 80 K to check whether the sample survived the cooling process. Additional measurements were taken above ambient (up to 335 K), to see how the sample would respond to higher than ambient temperatures.
Chapter 3: Results

3.1 Overview

Using the previously specified procedures, functional transistors were fabricated. These transistors were then characterized with the also aforementioned procedures. The results can be split into two groups: room temperature results and variable temperature results.

3.2 Room Temperature Results

The majority of the data resulting from this project was taken at room temperature. The differences between the transfer characteristics of Fe-OFETs and previously fabricated OFETs is illustrated in Figs. 3.1 and 3.2.
Figure 3.1: Transfer characteristics of a sample OFET.
Figure 3.2: Transfer characteristics of a sample Fe-OFET.

The hysteresis present in the transfer curve of the ferroelectric transistor that sets it apart from the ordinary OFET is due to the dipolar nature of the dielectric layer. Initially, when the gate voltage sweep is started at 25 V, the dielectric layer is unpolarized, so the current remains rather low. When the gate voltage reaches the proximity of zero voltage, the transistor starts to turn on. Here, the negative potential begins to polarize the ferroelectric dielectric layer due to the electric field it induces in this layer. Thus, the current increases from the combination of both the linear polarization and the ferroelectric polarization. 
of the transistor. When the maximum gate voltage is reached and the voltage sweep is reversed, the polarization state of the ferroelectric material does not change. Because the ferroelectric layer is more polarized by this point than it was while the voltage swept in the negative direction, the current is higher on the sweep in the positive direction than it was on the sweep in the negative direction. Just beyond when the voltage crosses zero for a second time, the ferroelectric dielectric layer becomes unpolarized again [14]. As the voltage returns to its starting point, the current returns to approximately where it started. One might expect that the transistor would transition into the opposite polarization state towards the end of the reverse sweep, but this is not the case as the use of gold for the source and drain contacts is not conducive to the injection of electrons into the transistor channel, and without the presence of bias electrons it is impossible for a polarization state of the P(VDF-TrFE) layer to remain stable at positive gate bias [14]. This is evidenced by the fact that two consecutive measurements yield the same result. If the second measurement started with the P(VDF-TrFE) layer in a polarized state compared to the unpolarized state at the start of the first measurement, one would expect to see differences in the second measurement. The disparity in the forward and reverse sweeps is most distinct at zero gate bias, when the source-drain current differs by about four orders of magnitude between the polarized and unpolarized states.

The performance of the transistors measured at room temperature was evaluated based on two metrics: yield and linear mobility. Yield is a fairly straightforward metric and reflects the overall quality of the fabrication process. In total, 40 transistors across
two samples were measured at room temperature. Within these two samples, the yield was 80%. The other performance metric, linear mobility, measures the speed at which charge carriers can move across the transistor channel while in the linear regime, defined as when the $V_d \ll V_g$. The mobility can then be estimated using the following expression for the current in the linear regime:

$$I_{SD} = \frac{W \mu C}{L} (V_G - V_T)V_{SD}$$  \hfill (3.1)$$

Next plot the source-drain current vs gate voltage and extract the slope under the linear regime, as illustrated in Fig. 3.3.
Using the slope of the plot of source-drain current vs gate voltage, it is found that that:

\[
\text{Slope} = \frac{W \mu CV_{SD}}{L} \tag{3.2}
\]

Which leads for the following expression for linear mobility:

\[
\mu = \frac{L \cdot \text{Slope}}{WCV_{SD}} \tag{3.3}
\]
Here $W$ is the channel width (1000 microns), $L$ is the channel length (30 microns) and $C$ is the capacitance of the dielectric layer. Calculating a value for $C$ adds significant complications to this process. During this project, it was impossible to measure the capacitance of a capacitor with a 1200 nm layer of P(VDF-TrFE) stacked on top of a 100 nm layer of CYTOP. To account for this lack of data, the capacitance was instead estimated based on calculated capacitances for each of the two dielectric layers according to the following equation:

$$\frac{1}{C_{\text{eq}}} = \frac{1}{C_{\text{CYTOP}}} + \frac{1}{C_{\text{Solvene}}}$$

(3.4)

$C_{\text{CYTOP}}$ can be easily estimated based on its linear dielectric constant, but extra care must be taken when calculating $C_{\text{Solvene}}$ because of the variable polarization of the P(VDF-TrFE) layer. $C_{\text{Solvene}}$ is estimated based on data provided by Richards Miller from a 260 nm thick P(VDF-TrFE) capacitor with an active area of 0.09 cm$^2$ [4]. From the capacitance vs voltage graph in Fig. 1.2, it is seen that the polarization switches at $V = \pm 20$ V. Assuming that maximum charge carrier density is the same for this capacitor as it is at the maximum polarization of the P(VDF-TrFE) layer of the transistors, it is possible to estimate the capacitance of the P(VDF-TrFE) layer in the transistors. Using equation 3.4, the equivalent capacitance for both dielectric layers is estimated to be 5.1 nF/cm$^2$. Using equation 3.3 to estimate the linear mobility of the 32 functional Fe-OFTEs, the mean linear mobility of the 32 functional transistors is found to be 0.015 cm$^2$/V*s. The maximum measured linear mobility was 0.18 cm$^2$/V*s. Notably, the results from one of the samples measured was much better than the other. The first sample measured had a yield
of 65% and a mean linear mobility of 0.0021 cm$^2$/V*s. The second sample had a yield of 95% with a mean linear mobility of 0.023 cm$^2$/V*s.

To understand why these mobility values are so low, it can be helpful to compare the calculated linear mobility values to saturation mobility values calculated for these same transistors. Two of the 40 transistors had measurements taken in the saturation regime ($V_g < V_d$). While this is an incredibly small sample, it can act as a litmus test for what might be going on with the transistors. In the saturation regime, the source-drain current in a transistor can be modeled using the following equation:

$$I_{SD} = \frac{W\mu C}{2L}(V_G - V_T)^2$$

The slope of the square root of the source-drain current is plotted vs the gate voltage, and the slope is extracted similarly to above, as shown in Fig. 3.4.
Figure 3.4: Extracting the slope for saturation mobility calculations. Note this is the same transistor as in Fig. 3.3.

From the slope of this plot, the following expression to estimate the saturation mobility can be extracted:

\[ \mu = \frac{2L \cdot \text{Slope}^2}{WC} \]  

(3.6)

Using this expression with the two transistors measured in the saturation regime, it was found that in both cases the saturation mobility was either around the same magnitude or greater than the previously calculated linear mobility, up to approximately twice as large.
Given that the linear mobility and saturation mobility should be about the same, this supports the notion that there may be contact effects acting at interfaces between layers in the transistors and negatively impacting their performance. The most likely candidate for the interface that is detrimental to transistor performance is the interface between the CYTOP and P(VDF-TrFE) layers of the transistors. One troublesome characteristic of P(VDF-TrFE) films is that they are typically quite rough. This is detrimental to charge transport because the roughness of the film means that at a local level, microcrystals of P(VDF-TrFE) do not align well [11]. This causes fluctuations in the polarization of the ferroelectric dielectric layer, which decreases the rate at which charge carriers can cross the channel. The roughness of materials such as P(VDF-TrFE) can be decreased through annealing at higher temperatures; however, this was not an option with the transistors fabricated in this project given that going much higher than 60 °C would damage the C8-BTBT semiconducting layer in the transistors. This roughness was expected to be an issue, which is one of the reasons the CYTOP layer was deposited between the C8-BTBT and the P(VDF-TrFE). It appears that either CYTOP is not well-suited for this application, or the layer was of an incorrect thickness for its intended purpose.

### 3.3 Variable Temperature Results

During this project, it was only possible to measure one Fe-OFET under varying temperatures. Because of this, it was necessary to rethink the role of the variable temperature measurements in this project. It is safe to say that no concrete conclusions can be inferred
from one transistor, so the following results are presented in the capacity that they serve as a baseline for further exploration.

Figure 3.5: Current vs temperature with voltage sweeping from positive to negative.
Figure 3.6: Current vs temperature with voltage sweeping from negative to positive.

The temperature dependent nature of charge transport in the transistor measured is first shown in Figs. 3.6 and 3.5 with plots of the source-drain current vs temperature for with the voltage sweeping from negative to positive and positive to negative, respectively. These plots both show a mostly exponential dependence of source-drain current on temperature. Note here that the above-room-temperature measurements shown here are from after the sample was cooled down to 80 K and returned to room temperature, a fact that will become relevant shortly. The linear mobility of charge carriers in the transistor was
calculated as in the previous section and is shown plotted vs temperature in Fig. 3.7.

![Linear Mobility vs Temperature](image)

Figure 3.7: Linear mobility values plotted vs temperature while decreasing and increasing temperature. Also shown is the mobility the day before the temperature experiment.

This mobility mirrors the exponential temperature dependence seen with source-drain current. It should also be noted that the mobility does not return to its original value when the temperature returns to room temperature, raising questions as to whether the transistor recovers from the cooling process. This prompts the following comparison between the transfer curves at several temperatures during the cool and heating stages of the temperature experiment.
Figure 3.8: Comparing the transfer curves of the transistor at 120 K before and after the cooling process.
Figure 3.9: Comparing the transfer curves of the transistor at 200 K before and after the cooling process.
Figure 3.10: Comparing the transfer curves of the transistor at 295 K before and after the cooling process.
Comparing transfer curves, the source-drain current while in the cooling stages of the temperature experiment is universally higher than in the heating phase. Moreover, it is apparent that the hysteresis at 295 K is significantly less noticeable after heating all the way up to 295 K when compared to the start of the temperature experiment. This suggests that the transistor changed in some way during the heating and cooling process. The P(VDF-TrFE) layer appears to be a likely candidate for the location of this change, given the reduction in hysteresis from the start to the end of the experiment. Alternatively, it is also possible that the probes made worse contact with the contacts on the transistor in the heating phase, which would also explain the reduced current. Another interesting observation from the previous plots is that the hysteresis present at room temperature disappears when the sample is cooled, suggesting that the P(VDF-TrFE) might change phases at lower-than-ambient temperatures. Additional data would need to be collected to either confirm or deny this possibility, as the apparent reduction in hysteresis could result from the worsening of contact effects at lower temperatures. Given the suspected disorder of the P(VDF-TrFE) layer caused by its roughness, it might also be the case that lower temperatures simply prevent domains in this ferroelectric layer from orienting their dipole moments in the same direction, thus preventing the P(VDF-TrFE) film from being significantly polarized in either direction under these conditions. A possible explanation for why these domains are unable to orient their dipole moments in the same direction is that individual polymer chains in the P(VDF-TrFE) layer might be harder to polarize at lower temperatures [15].
From the time when the transistors were first measured in air at room temperature to when the temperature experiment was conducted one day later, the performance of the transistor measured in the temperature experiment dropped dramatically. This is evidenced by Fig. 3.7 which demonstrates the decrease in linear mobility exceeding an order of magnitude. Comparing transfer curves between the two days sheds some insight into why this might be the case.

Figure 3.11: Transfer curves from the day before and the day of the temperature experiment.
Clearly, the source-drain current is much higher at most of the gate voltage sweep the day before the temperature experiment in air when compared to measurements taken the day of the temperature experiment under vacuum; however, one notices that the current when the ferroelectric dielectric layer is unpolarized is very similar in either case. It is just when the ferroelectric polarization switches to the polarized state that the current tends to be lower than the day before. This supports the notion of the existence of an aging effect influencing the P(VDF-TrFE) layer in some way.

As with the room temperature results, there are considerable caveats associated with the results of the temperature experiment. The linear mobility was even lower than the average linear mobility of the room temperature samples even at 295 K, and this problem was worsened as the temperature decreased. This low performance was likely due to similar contact effects as seen above, which tend to be exacerbated by low temperatures. Furthermore, it was impossible to account for the possible change in dielectric constant due to changing temperatures, which could have played a significant role in the behavior of the transistor observed at low temperatures.
Chapter 4: Conclusions

In this project, previously established experimental methodologies were adapted to fabricate a transistor type so far unexperimented with in the UVM Physics Department. These experimental procedures were successfully implemented, resulting in functional top-gate, bottom-contact ferroelectric organic field effect transistors. The measurement of these transistors, both in air at room temperature and in vacuum under varying temperatures led to estimates of charge carrier mobility for these transistors in the linear regime. These results are reflective of imperfections in the nascent fabrication procedure used. The transistors did display significant hysteresis as is characteristic of Fe-OFETs, with differences in current between the polarized and unpolarized states of the ferroelectric dielectric layer of up to four orders of magnitude. This hysteresis shows that the transistors fabricated have potential as non-volatile memory devices. Overall, this project lays out a foundation on which can be refined to achieve better results. Given the numerous real-world applications of Fe-OFETs such as the aforementioned non-volatile memory, the continuation of this research certainly seems worthwhile.
Chapter 5: Future Recommendations

The baseline established in this project provides significant avenues within which this research could be continued and improved. Primarily, further research should attempt to improve Fe-OFET performance. The two areas in the experimental methodology that appear to contain the most potential for improvement are the semiconducting films and the interfaces between the ferroelectric layer and its surrounding layers. The fabrication of the semiconducting layer was not a primary focus in this project, a fact that is reflected in the lack of consistency in performance between samples. One definite pathway to increased performance exists in an experiment quantifying the impact of the exact deposition conditions of microslot-written C8-BTBT on the characteristics of the resulting films.

Not enough samples were fabricated in this project to optimize the ferroelectric dielectric layer in the transistors or the adjacent CYTOP buffer layer. Improving this P(VDF-TrFE) layer could be approached from a number of angles. The first would be to decrease the roughness of the P(VDF-TrFE) layer directly. This could come as the result of optimizing the deposition conditions of P(VDF-TrFE). More likely, however, decreasing roughness would require annealing at a higher temperature. Higher temperature annealing could be allowed in two manners. The first would be to retain the same transistor architecture but replacing the C8-BTBT used with a semiconducting material that capable of withstanding higher temperatures. If it was desirable to continue using C8-BTBT as the semiconductor material, the transistor architecture could be swapped from a top-gate, bottom-contact configuration to a bottom-gate, top-contact architecture. This swap would allow the di-
electric to be annealed at a higher temperature before the C8-BTBT film was written; however, it would also bring with it a whole slew of other design challenges. The other option would be to explore alternative buffer layers. CYTOP might not be the best option in this regard, and so other materials such as Poly(methyl methacrylate)(PMMA) could be considered as potential alternatives.

The other avenue for future research is in the progression of experimental methodologies outlined in the project towards commercial viability. Given the application of the Fe-OFETs fabricated in this experiment as non-volatile memory, Fe-OFETs made in future studies should be benchmarked in additional metrics that are relevant in memory applications such as the time required to switch between polarization states, and the time an Fe-OFET can retain its polarization state. Finally, further studies could consider the up-scaling of the fabrication process from the small 15 mm by 20 mm substrates used in this experiment to larger substrates that would be more typical of an industrial production line. This transition could also be coupled with the switch to flexible substrates, which are relevant in many portable electronics applications. Using flexible substrates would necessitate the use of a platform for solution processing such as the roll coater illustrated in Fig. 5.1.
Figure 5.1: Roll coater which could be used to upscale transistor fabrication.

This transition would certainly not be without challenges. It is impossible to spin-coat layers on the larger-surface area, thinner substrates used with the roll coating platform. This means that it would be necessary to validate the performance of microslot or slot-die written CYTOP and P(VDF-TrFE) films for this transition to be deemed successful. However, given that samples fabricated on these substrates would be far closer to what real world applications of Fe-OFETs might look like, overcoming these challenges is a worthwhile undertaking.
Bibliography


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