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CMOS PROGRAMMABLE TIME CONTROL CIRCUIT DESIGN FOR PHASED
ARRAY UWB GROUND PENETRATING RADAR ANTENNA BEAMFORMING

A Thesis Presented

by

Nicholas Reilly

to

The Faculty of the Graduate College

of

The University of Vermont

In Partial Fulfillment of the Requirements
For the Degree of Master of Science
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ABSTRACT

Phased array radar systems employ multiple antennas to create a radar beam that can be steered electronically. By manipulating the relative phase values of feeding signals among different antennas, the effective radiation pattern of the array can be synthesized to enhance the main lobe in a desired direction while suppressing the undesired side lobes in other directions. Hence the radar scanning angles can be electronically controlled without employing the bulky mechanical gimbal structure, which can significantly reduce radar system size, weight and power consumption. In recent years, phased array technologies have received great attentions and are explored in developing many new applications, such as smart communication systems, military radars, vehicular radar, etc. Most of these systems are narrow band systems, where the phase delays are realized with narrow band phase shifter circuits. For the impulse ground penetrating radar however, its operating frequency spans an ultrawide bandwidth. Therefore the traditional phase shifters are not applicable due to their narrow band nature. To resolve the issue, in this study, a true time delay approach is explored which can precisely control time delays for the feeding pulse signals among different antennas in the array. In the design, an on chip programmable delay generator is being developed using Global Foundry 0.18 μm 7 HV high voltage CMOS process. The time delay control is realized by designing a programmable phase locked loop (PLL) circuit which can generate true time delays ranging from 100 ps (picoseconds) to 500 ps with the step size of 25 ps. The PLL oscillator's frequency is programmable from 100MHz to 500MHz through two reconfigurable frequency dividers in the feedback loop. As a result, the antenna beam angle can be synthesized to change from 9.59° to 56.4° with a step of 2.75° , and the 3dB beamwidth is 10° . The power consumption of the time delay circuit is very low, where the supply voltage is 1.8V and the average current is as low as 472uA.

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1. Introduction

The primary motivation for this work is presented in this section.

1.1 Motivation

Ground penetrating radar (GPR) is useful for scanning bridges, roadways, and other subterranean structures and detecting their wear and erosion conditions. Traditional GPR systems emits radar pulse signals straight down, obtaining a 2D scan image of the subsurface object directly underneath. If a 3D scan of a larger area is desired, a traditional GPR system needs to take many passes over the area, spaced uniformly apart, and collects all the data to construct the 3D image. Such method is time consuming and computation intensive. Phased array radar allows the user to obtain 3D images by making less passes, and instead sweeping the radar beam electronically from side to side. In order to implement a phased array radar system, a beamforming control subsystem is required. Traditional phased array radar systems develop the phase offset using passive devices for each antenna element to steer the beam. However for ultra wide band (UWB) GPR, generating phase offsets directly becomes less practical, mainly due to the narrow band characteristics of traditional phase shifters. To resolve the issue, a true time delay unit is desired to steer the beam in UWB GPR array. In [8] more benefits of using a true time delay as opposed to a standard phase shift are discussed. The main is that with a phase offset that is set as a function of the operating frequency, the beamforming varies over changes in the frequency. When using true time delay as a function of the frequency, the

beamforming remains constant. Instead only the signal beam width is affected. These results are demonstrated in the Figure 1.1, below.

Figure 1.1: Comparison of Phase Shift and True Time Delay Beamforming with Respect to Operating Frequency [8].

Many phased array systems have been developed using the true time delay approach, such as [2] and [14]. These systems generally follow a similar design approach, using low voltage control circuitry to generate the time delays while relying on external pulse forming networks and power amplifiers to generate the high voltage radar pulses. The novelty in this research is that it uses a mixed power supply technology. Doing so allows the controls of the system to operate at a low supply voltage (1.8V), while also providing the capability to generate the high voltage GPR all on a single chip. The result is a complete phased array radar SOC (system on chip), as Figure 2.1 shows. The SOC allows for low power control with the ability to generate high amplitude pulses for increased ground penetrating depth on a single chip, which is not available in other current systems. By designing the system like so, the complexity of the GPR system is greatly reduced.

1.2 Phased Array Basics

Phased array radar systems eliminate the need for mechanical gimbal structures, which are used by many traditional radar systems to direct the power of the radar beam. They instead use an array of antennas to steer the beam electronically, by controlling the phase offset between the radar pulses sent out by each radiating element. The basic concept of phased array radar beamforming is shown in Figure 1.2.

Figure 1.2: UWB Beamforming [9].

The GPR system being developed will be towed behind a vehicle. If the vehicle will be traveling at any substantial speed, a 3D image would be impossible to obtain with a radar system that scans mechanically. By steering the beam electronically, the system is able to change the beam direction in a matter of microseconds, as opposed to mechanical gimbals, which are limited by the physical structure, and can normally change the beam direction on the order of milliseconds or more. The property of quick beam redirection is

the key advantage to phased array radar, and is the reason it is desirable for the system being designed.

Figure 1.3: GPR Scan Orientations [3].

Figure 1.3 demonstrates how the GPR system is used. It is towed behind a vehicle traveling in the X direction, while the radar beam is swept electronically back and forth in the Y direction. The data obtained is then used to reconstruct a 3D image of the ground below.

Because GPR uses an ultra wideband pulse, it is not practical to directly control the phase offset at each antenna. Instead, a true time delay method will be used. In true time delay phased array beamforming, a time delay is created between each of the trigger signals that are applied to the UWB pulse generators, before the pulses are created. The time delay then follows to the pulses themselves, creating an effective phase offset between each pulse. In [2], a true time delay beamforming subsystem is presented. The system

diagram from [2] is very similar to the system design of this project, and is shown in Figure 1.4.

Figure 1.4: System Diagram from [2].

The main difference is that this project contains the beamforming subsystem and the UWB pulse generators on the same chip, instead of using external pulse forming networks (PFN) to create the high power radar pulses. The measurement results from [2], shown in Figure 1.5. demonstrate that the beam radiation patterns match well with the theoretical calculations discussed in section 5.

Figure 1.5: Measured Scan Angles from [2] for 100 ps and 400 ps Delay.

The design in [2] proves the effectiveness of the true time delay beamforming system. However the system performance is constrained by beamforming resolutions due to coarse time delays created, where the time delay step size is 100 ps (picoseconds). This project builds off the true time delay method, but is designed in a way such that it can create delays in time steps of 25 ps. The fine delay tuning achieved leads to a much better scan angle resolution, resulting in better imaging resolution and overall radar system performance.

Some more complicated methods such as calibrated Vernier delay lines [14] have been used to generate more precise delays with the phase tuning step value as low as 10 ps. The delay line from one such system is shown in Figure 1.6. The downfall of these systems is that they are purely digital and operate with low supply voltages, presenting a need for off chip power amplifiers to create the UWB pulses that are sent through the antennas. These designs are also very complex in their nature, and are therefore the performance is very sensitive to PVT (process, voltage, temperature) variations.

Figure 1.6: Delay Line from [14].

Creating the UWB radar system as a system on chip (SOC) greatly simplifies the use of the system. All that is needed to operate the radar system designed here is two power supplies (one low voltage for control circuitry and one high voltage for pulse generation), a 20 MHz crystal oscillator, a differential pulse generator, and the antenna elements. Using a tunable PLL to control the delay provides the feedback mechanism required to ensure that the delays generated on the chip after fabrication operate as expected. It also

gives the capability to adjust the PLLs operating frequency as needed if the delays created differ from what is expected.

1.3 Thesis Organization

This thesis gives an overview of the UWB beamforming system that has been designed. First, it discusses how a programmable phase locked loop is used to generate the precise time delays that are required for this beamforming. The design and detailed operation of the components of the beamforming system are then discussed. From there, simulated results of the circuit are presented and reviewed. Then it gives a summary of the beamforming capabilities of a general phased array system, and discusses how these concepts apply to this system in particular. Next, it shows the theoretical beamforming performance that is achieved by this system. After, the chip layout and related metrics are discussed. It finishes with an overview of the planned future work that will be done to continue the UWB beamforming project.

2. System Overview

Figure 2.1: Full Beamforming System Diagram.

The overall system schematic that is used is shown in Figure 2.1. The most important element of the system is the programmable PLL, which is discussed in detail in section 2.1. This programmable PLL contains a voltage controlled oscillator (VCO), which is constructed as a ring oscillator using the exact same delay cells as the replica delay cells used to create the delayed trigger pulses that activate the pulse generators. The PLL is set to oscillate at a desired frequency, which correlates to a known delay Δt at each of the delay cells in the VCO, as discussed in section 2.3. The same control voltage that sets the delay for the delay cells in the VCO is also used to control the delay of the replica delay cells pictured here. These replica delay cells can then be fed a trigger pulse. The trigger pulse will propagate through each of the replica delay cells, creating a series of such

trigger pulses with a known delay of Δt between each of the rising edges. By changing Δt , the angular direction of the overall power of the constructed radar beam is changed. Control of Δt is what allows the beamforming to occur.

2.1 Overview of PLL

Figure 2.2: PLL Block Diagram.

The general block diagram for a programmable phase locked loop (PLL) is shown in Figure 2.2. It consists of a phase frequency detector (PFD), a charge pump, a low pass filter (LPF), a voltage controlled oscillator (VCO), and two frequency dividers. The reference frequency is generated with an off chip crystal oscillator, which operates at 20MHz. The reference signal is divided by K, and then fed to the PFD. The other input of the PFD is the divided output of the VCO. The function of the PLL is to drive these two signals such that they have zero phase offset. The PFD outputs *up* and *down* signals, which change duty cycle based on whether the frequency of the VCO needs to increase or decrease. When the *up* signal has a larger duty cycle, it causes the charge pump to sink current from the loop filter, decreasing the control voltage that is fed to the VCO, and therefore increasing its frequency. When the duty cycle of the *down* signal is larger, the charge pump will source current to the loop filter, which increases the control voltage, thus decreasing the frequency of the VCO. When the phase of the two inputs of the PFD

line up, the *up* and *down* signals will have the same duty cycle, and the charge pump sources and sinks the same amount of current from the loop filter, causing the control voltage to remain constant.

2.2 Relation between Locking Frequency and Delay

The VCO used is comprised of ten of the differential delay cells, connected in a ring oscillator configuration. Because of this, the signal must propagate through the chain of ten cells twice in order to create one full period at the output. Using the topology described gives the following relationship between the delay of one cell, Δt , and the overall period at the output of the VCO, T

$$T = \Delta t * 20 \quad (2.1)$$

Inverting Equation (2.1) shows the relationship between the delay and F_{VCO}

$$F_{VCO} = \frac{1}{(\Delta t * 20)} \quad (2.2)$$

We can finally rearrange Equation (2.2) in a way that clearly shows what Δt will be created for a particular value of F_{VCO}

$$\Delta t = \frac{1}{(20 * F_{VCO})} \quad (2.3)$$

These equations are used to determine what frequencies the VCO must oscillate at to achieve the desired delay over each delay cell in the VCO. The results are summarized in Table 1.

Table 1: Loop Frequencies and Respective Delays Achieved

Fvco (MHz)	Delay (ps)
500	100.00
400	125.00
330	151.52
285	175.44
250	200.00
220	227.27
200	250.00
180	277.78
166.67	300.00
153.33	326.09
143.33	348.84
133.33	375.00
125	400.00
117.5	425.53
110	454.55
105	476.19
100	500.00

It can be seen from Table 1 that the step between two successive delays is not always exactly 25 ps. The variation is due to the resolution of the frequency dividers used. As long as the delay is known, however, these slight variations in delay resolution can be accounted for, and do not affect system performance.

Because the replica delay cells that are used to create the actual trigger pulses are the same as those used in the VCO, and the control voltage used to bias them is the same, the

same delay Δt is observed at these replica delay cells as well. The relationship between the period at the output of the VCO and the delay of each cell is discussed in more detail in section 3.3. The next section discusses how the two programmable frequency dividers are used to set the VCO to operate at the frequencies shown in Table 1.

2.3 Programming with Frequency Dividers

Two programmable frequency dividers are used in the design. One is used as a prescaler, where its function is to cut down the frequency of the off chip reference signal, allowing access to multiple reference frequencies that can be fed to the PLL. The other divider is the in loop divider, which divides down the high frequency of the VCO output to a value that can be compared with the reference frequency. The setup of these dividers is shown in Figure 2.3. For the remainder of the paper, the divide by modulus of the prescaler is referred to as K, and the divide by modulus of the in loop divider is referred to as N.

Figure 2.3: Use of Frequency Dividers in this System.

The function of the PLL is to drive the phase, and therefore frequency of the two inputs to be equal. When the dividers are considered, it results in the following equation

$$\frac{F_{ref}}{K} = \frac{F_{VCO}}{N} \quad (2.4)$$

Equation (2.4) can then be rearranged to the following format, which demonstrates how the two dividers are used with a constant F_{ref} to set F_{VCO} to a desired value.

$$F_{VCO} = F_{ref} * \frac{N}{K} \quad (2.5)$$

The value N/K is referred to as the divide ratio. Using Equation (2.5) and a constant $F_{ref} = 20\text{MHz}$ gives way to Table 2, that demonstrates what divide values are needed to set F_{VCO} to all of the values that will be used to create the delays, as discussed in section 2.2.

Table 2: Frequency Divider Values Used to Generate Desired Frequencies

Loop Divider (N)	Prescaler (K)	Ratio	Fvco (MHz)	Delay (ps)
50	2	25.00	500	100.00
40	2	20.00	400	125.00
33	2	16.50	330	151.52
57	4	14.25	285	175.44
50	4	12.50	250	200.00
44	4	11.00	220	227.27
40	4	10.00	200	250.00
36	4	9.00	180	277.78
50	6	8.33	166.67	300.00
46	6	7.67	153.33	326.09
43	6	7.17	143.33	348.84
40	6	6.67	133.33	375.00
50	8	6.25	125	400.00
47	8	5.88	117.5	425.53
44	8	5.50	110	454.55
42	8	5.25	105	476.19
40	8	5.00	100	500.00

3. Delay Control Circuit Design Based on PLL

3.1 Overall System Design

Figure 3.1: Full Beamforming Subsystem Schematic.

The full schematic for the beamforming subsystem is shown in Figure 3.1. The delay is controlled with the programmable PLL, shown in the bottom half of the figure. It is programmed by changing the values of the Control_0 and Control_1 inputs, which set the divide ratios for the two frequency dividers. Setting these values sets the loop to oscillate at a certain frequency, as described by section 2.3. The same control voltage used to control the VCO is also fed to the replica delay cells, pictured in the upper half of the figure. Because the control voltage is the same, the loop frequency is directly related to the delay of the replica delay cells by Equation (2.3), as section 2.2 describes. Once the

loop has reached its locked state, a differential trigger pulse is applied. The pulse then propagates through the replica delay cells, creating the delay that is desired. The differential output of each of the delay cells is connected to a differential to single ended converter, which create the full swing trigger pulses separated by the set delay. These trigger pulses are then used to activate the high voltage pulse generators, which will also be contained on the same chip, but are out of the scope of this research. The pulses created by these pulse generators will be fed directly to the antenna elements of the radar system. The receiver circuitry will be housed on the same chip as well, but that is also out of the scope of this project. The result of this configuration is that the entire phased array radar system is on a single chip (SOC). The remainder of section 3 discusses the individual components of the system in further detail.

3.2 Delay Cell and Biasing Circuit

Figure 3.2: Schematic of Differential Delay Cell.

The design of a differential delay cell and biasing circuit is shown in Figure 3.2. Its design is adopted from [9]. The delay cell is capable of generating time delays ranging from 58 ps up to 8.1 ns, although only delays in the range of 100 to 500 ps will be used. The delays increase exponentially as a function of the control voltage. The control voltage and time delay characteristic is plotted in in Figure 3.3.

Figure 3.3: Delay Characteristic of Differential Delay Cell.

The delay of the cell is controlled by two bias voltages, V_{bp} and V_{bn} . The bias voltage V_{bp} is a noise immune version of V_{ctrl} , created by the bias generator. Its function is to

change the effective resistance of the symmetric load element created with transistors TP3 and TP4. The change in resistance changes the RC constant of the cell, which causes the delay to change. Transistor TN3 is a controlled current source that is biased with Vbn, which allows the cell to compensate for drain and substrate voltage variations.

Figure 3.4: Biasing Circuit Schematic.

The biasing circuit, shown in Figure 3.4, takes the control voltage and generates the bias gate voltages for the NMOS and PMOS biasing transistors of the delay cell. Its main function is to continuously adjust the buffer bias current in order to provide the proper lower swing limit of the control voltage to the delay stages. It does so with a differential amplifier and half buffer replica. Transistors TP0, TP1, and TN1-4, create the bias for the differential amplifier which is comprised of transistors TP2-4, TN5 and TN6. TP5, TP6, TN7, and TN8 make of the half buffer replica; while TP7, TP8, TN9, and TN10 act

as a final buffer to the bias voltages. The circuit described allows the bias generator to establish a current for these bias signals that is held constant and independent of the supply voltage. Using the biasing circuit increases the immunity of the control voltage to supply noise. All of the internal biasing voltages and currents are generated from each other, meaning that the bias levels are determined completely by the operating conditions [9]. The biasing circuit also isolates the control voltage from being directly attached to the delay cells in the VCO. It prevents any capacitive coupling that could otherwise introduce high frequency noise into the control voltage.

Figure 3.5: Control Voltage and Corresponding Bias Voltages when PLL is set to 100MHz.

Figure 3.5 shows how the two bias voltages respond to changes in the control voltage. They do not vary as much as the control voltage does when current is injected into the loop filter. The smoothing of the signals is due to the added capacitance from the transistors used in the bias cell, as well as capacitors C_n and C_p . V_{bp} tracks V_{ctrl} fairly closely, while V_{bn} settles to a much lower value, adjusting the current of the controlled current source to its proper value. The capacitors attached to the output of the circuit also help to filter out the majority of the high frequency control voltage jitter, so it does not transfer to these bias signals. Adding the capacitors greatly increases the accuracy of the delays that are created by the replica delay cells. The next section discusses how these delay cells are used to create the VCO that is used in the PLL.

3.3 Voltage Controlled Oscillator

Figure 3.6: Voltage Controlled Oscillator Using Differential Delay Cells.

The voltage controlled oscillator is comprised of ten differential delay cells, hooked up in a ring oscillator configuration. The positive output of one delay cell is attached to the positive input of the next, and the same is done with the negative inputs and outputs, all

the way up to the tenth cell. For the last cell, its positive input is attached to the negative input of the first cell, and vice versa, as the figure shows. Doing so is what allows an even number of delay cells to be used. Using the topology shown leads to the relationship between the delay of one cell, Δ , the number of cells used, and the period of the VCO output, T

$$T = \Delta * 2 * n, \quad n = 2, 4, 6, \dots \quad (3.1)$$

In the design, 10 delay cells are used in the ring oscillator, leading to the final equation

$$T = \Delta * 20 \quad (3.2)$$

Equation (3.1) differs from a standard inverter ring oscillator because it requires an even number of delay elements to function. The control voltage to frequency of oscillation characteristic is shown in Figure 3.7.

Figure 3.7: VCO Frequency related to Control Voltage.

From Figure 3.7 it can be seen that the frequency of oscillation decreases as the control voltage increases. The inverse relationship is due to the voltage to delay characteristic shown in Figure 3.3. The delay over one cell increases as the voltage decreases, and the longer delays cause the VCO operating frequency to decrease. Figure 3.7 also shows that the frequency varies linearly for control voltages in the range of .1V to 1.2V, at which point it begins to flatten off. The minimum frequency of the VCO is 6.2MHz, but it is not shown in the figure since it is out of the frequency range that will be used. This corresponds to the maximum delay of 8.1 ns over each delay cell.

3.4 Frequency Dividers

As discussed in section 2.3, two frequency dividers are used in the design. The prescaler design is shown in Figure 3.8.

Figure 3.8: Prescaler Frequency Divider Schematic.

The prescaler divider consists of a three bit counter, a three bit comparator, and a T flip flop. The user sets a three bit binary number, and the value of that number corresponds to $\frac{1}{2}$ the divide value K. The counter counts from 0 up to 7 in binary, and the comparator compares the output of the counter with the user set value. When these values are equal, the comparator output will go high. This causes the T flip flop to change states, and also resets the counter. The T flip flop must change states twice to get one period of the output frequency, which leads to the relationship between the set value and K as mentioned previously. The divider described is capable of setting K values from 2 up to 14 in steps of 2. Three bit components are used to give access to the range of K values required as defined by Table 2.

Figure 3.9: Schematic of Multi-Modulus Divider.

For the in loop divider, it adopts the multi-modulus design scheme [13] that is capable of generating divide values ranging from 2^n to $2^{n+1}-1$, where n is the number of 2/3 divider circuits used. Figure 3.9 illustrates the divider circuit diagram that is constructed by a chain of serially connected 2/3 divider circuit elements. The divide value N is set with the control inputs, and is governed by the following equation

$$N = 2^n + Con_0 2^0 + Con_1 2^1 + \dots + Con_{n-1} 2^{n-1} \quad (3.3)$$

In this system, $n = 5$, generating divide values that range from 32 to 63 in integer increments.

Figure 3.10: Logic Diagram of Divide by 2/3 Circuit.

Figure 3.10 shows the logic diagram of the divide by $2/3$ circuit used. The output of the circuit has a period that is double the period of the input, unless *Control* and *MODin* are both logic one, making the output period triple the input. The *MODout* signal has the same period as the output, but a different duty cycle. It is connected to the *MODin* of the previous divider in the chain. That signal is logic one for only one input cycle of the next divider, adding an extra input cycle to the output provided *Control* is high, and setting the instantaneous divide ratio to 3. Thus the ratio can be changed by only setting the *Control* inputs of each divider.

Figure 3.11: Operation of Multi-Modulus Divider when set to $N = 32$.

Figure 3.11 shows the input and output signals of the multi-modulus divider, as well as all of the mod signals and intermediate frequencies, when set to divide by 32. That ratio corresponds to all control bits being set to 0, and all cells dividing by two. As the figure shows, the mod signal is only high for one output cycle of the previous divider. If the control signal is high for any one of the dividers, it divides by three for only one of the cycles of its output. That is what creates the relationship described in Equation (3.3).

3.5 Phase Frequency Detector

Figure 3.12: NOR Gate Based Phase Frequency Detector Using D Flip-Flops

Figure 3.13: Phase Frequency Detector Used in this Design.

A simple CMOS PFD is used [11]. It's operation logic is the same as a standard PFD created with two D flip-flops and a NOR gate, as shown in Figure 3.12. The schematic for the PFD that is used is shown in Figure 3.13. Transistors TP3 and TN2 create an

inverter that is only activated when the F_{ref} signal is low, turning on TP1. TP2 and TN1 also create an inverter, which is only activated when F_{ref} is high, turning on TN3. The configuration described simulates an edge triggered D flip-flop with its input tied to logic 1. The transistors in the right half of the circuit operate in an identical fashion, except they are activated by F_{in} instead. The purpose of the PFD is to generate differential up and down pulses, which vary in width based on the difference in the rising edges of the input signals. Using the design from [11] allows the PFD to be created with only 24 transistors, as opposed to the 80 that would be required if full D flip-flops were used. The PFD design used has been shown to produce a small dead zone and low jitter [11]. A simulated result of the operation of the PFD is shown below.

Figure 3.14: PFD Signal Operation During Loop Transient State.

Figure 3.14 demonstrates the signal operation of the PFD while the loop is in its transient state. As the figure shows, when the rising edge of the reference signal comes before the rising edge of the input signal, the *up* signal goes high. This signifies that the input frequency needs to increase in order to line up with the reference frequency. The *up* signal will stay high until a rising edge of the input signal is seen, at which point this

signal falls low again. If a rising edge of the input signal is seen first, the *down* signal goes high. The *down* signal will in turn stay high until a rising edge of the reference signal is seen, signifying that the input frequency needs to decrease to line up with the reference. The next figure demonstrates how the PFD operates with in phase inputs.

Figure 3.15: PFD Signal Operation with In-Phase Inputs.

Figure 3.15 shows simulated results of how the PFD will operate when both the F_{ref} and F_{in} signals are in phase with each other. The up and down signals remain low, except for a short duration pulse during the rising and falling edges of the signals. Because of the presence of these pulses, the charge pump is designed in such a way that it sources and sinks the same amount of current, preventing net charge from being transferred to the loop filter when the two signals are locked. If this were not the case, large jitter would occur and the loop would never fully reach its locked state. The next section describes how the charge pump is designed to achieve this.

3.6 Charge Pump

The up and down signals that are the outputs of the PFD are fed to the charge pump inputs. They cause the charge pump to source and sink current, depending on which

signal is high. The current charges and discharges the loop filter capacitor, continually adjusting the control voltage until the PFD inputs are in phase. Because the PFD outputs even duration pulses when the inputs are in phase, it must be ensured that the positive and negative charge pump currents are equal in magnitude.

Figure 3.16: Differential Charge Pump.

The differential charge pump circuit used is shown in Figure 3.16. The design is adopted from [9]. It consists of two NMOS source coupled pairs, each with their own current source. The current source is biased with the same bias voltage that controls the current source of the delay cells, V_{bn} . These pairs are connected by a current mirror, constructed from symmetric load elements. Charge will be transferred from the loop filter when the Up input is high, and to the loop filter when the Down input is high. When both Up and Down inputs are high, the PMOS in the right source coupled pair has V_{ctrl} at its gate and drain, and sources the same buffer bias current that is sunk by the remainder of the source

coupled pair [9]. By doing so, it can be ensured that no net charge is transferred to the loop filter when the PFD inputs are in phase, allowing the control voltage to settle to a stable value with very little jitter.

3.7 Loop Filter

A second order low pass filter is used as the loop filter in the PLL. The general topology of one such filter is shown in Figure 3.17, below.

Figure 3.17: 2nd Order Low Pass Filter.

The transfer function of the filter is given by

$$Y = \frac{sC_2(sC_1R + 1) + sC_1}{sC_1R + 1} \quad (3.4)$$

In order to properly determine the values of the components for the loop filter, the transfer function of the full PLL is studied.

Figure 3.18: Simplified PLL in Frequency Domain [12]

Figure 3.18 shows the frequency domain representation of a simplified PLL as discussed in [12]. The transfer function for the simplified PLL is given as

$$\frac{\theta_0(s)}{\theta_R(s)} = \frac{\frac{A_0 K_{phase} F(s)}{N} * \frac{K_{VCO}}{s}}{1 + \frac{A_0 K_{phase} F(s)}{N} * \frac{K_{VCO}}{s}} \quad (3.5)$$

In Equation (3.5), A_0 is the DC gain of the loop filter, K_{VCO} is the gain of the VCO, $F(s)$ is the impedance of the loop filter, and K_{phase} is the gain of the PFD and charge pump combined, which is written as

$$K_{phase} = \frac{I_{CP}}{2\pi} \quad (3.6)$$

Equation (3.5) can then be simplified to the form

$$\frac{\theta_0(s)}{\theta_R(s)} = \frac{kF(s)}{s + kF(s)} \quad (3.7)$$

Where k is the following

$$k = \frac{A_0 K_{phase} K_{vco}}{N} = \frac{A_0 I_{CP} K_{VCO}}{2\pi * N} \quad (3.8)$$

In general, A_0 is assumed to be 1, since there is no DC gain in the loop filter. For the purpose of analysis, it is acceptable to ignore C_2 in the loop filter equation, as it is generally set to one tenth the value of C_1 and will not have a significant impact on loop stability. The function of C_2 is to add a high frequency pole to the transfer function, helping to remove high frequency ripple on the control line. Thus the impedance of the loop filter can be approximated as

$$F(s) = \frac{sC_1 R + 1}{sC_1} \quad (3.9)$$

Combining the results of Equations (3.7), (3.8) and (3.9) leads to the following transfer function for the full loop

$$\frac{\theta_0(s)}{\theta_R(s)} = \frac{\frac{I_{CP} K_{VCO}}{2\pi * N * C_1} * (RC_1 s + 1)}{s^2 + \frac{I_{CP} K_{VCO}}{2\pi * N} * R * s + \frac{I_{CP} K_{VCO}}{2\pi * N * C_1}} \quad (3.10)$$

Which takes the form

$$\frac{\theta_0(s)}{\theta_R(s)} = \frac{\omega_n (\frac{2\xi}{\omega_n} s + 1)}{s^2 + 2\xi \omega_n s + \omega_n^2} \quad (3.11)$$

By comparing (3.11) and (3.12), it can be seen that the natural frequency and damping factor for the transfer function are given by Equations (3.11) and (3.12), respectively

$$\omega_n = \sqrt{\frac{I_{CP}K_{VCO}}{2\pi * N * C_1}} \quad (3.12)$$

$$\xi = \frac{R}{2} \sqrt{\frac{I_{CP}K_{VCO}C_1}{2\pi * N}} \quad (3.13)$$

A useful design strategy is to choose the values of ω_n and ξ first, and then based on these desired values calculate the values of R and C_1 . Equations (3.11) and (3.12) can be written in the following format to allow this.

$$C_1 = \frac{I_{CP} * K_{VCO}}{2\pi * N * \omega_n^2} \quad (3.14)$$

$$R = 2\xi \sqrt{\frac{2\pi * N}{I_{CP} * K_{VCO} * C_1}} \quad (3.15)$$

A common design choice is to choose the damping factor ξ to be .707, as doing so leads to a quick locking time for the system. The 3dB cutoff frequency is chosen to be one tenth the reference frequency. In this system the reference frequency is 20MHz, leading to a 3dB cutoff frequency of 2MHz. The natural frequency of the system can then be calculated using the approximation from [12]

$$\omega_n = \frac{\omega_{3dB}}{(1 + \xi\sqrt{2})} \quad (3.16)$$

When ξ is chosen to be .707, the natural frequency turns out to be half the 3dB cutoff frequency, giving ω_n a value of $2\pi \cdot 1\text{MHz}$ in this system. The charge pump current I_{CP} is set to approximately $20\mu\text{A}$, and the gain of the VCO K_{VCO} is measured to be 708.31MHz/V . The value of N in the system designed actually corresponds to N/K , as that is the effective divide ratio when two frequency dividers are used. Its value ranges from 5 up to 25, so the median of 15 is chosen for these calculations.

Using these values and Equation (3.13), the value of C_1 is calculated to be 3.923pF . Dividing the value of C_1 by ten gives a value for C_2 of 392.3fF . When plugging these values into Equation (3.14), a value of $R = 57.365\text{k}\Omega$ is calculated. Due to the physical limitations of the cadence program, these exact values could not be used. Table 3 summarizes the actual values that were used in the loop filter.

Table 3: Calculated Loop Filter Values and Actual Values Used

Component	Calculated Value	Value Used	Difference
R1	57.365k Ω	57.343k Ω	22 Ω
C1	3.923pF	3.9215pF	1.5fF
C2	392.3fF	392.19fF	.11fF

3.8 Differential to Single Ended Converter

The UWB pulse generator circuit that is used is triggered with a full swing steep transition single ended signal. The differential delay cells that are used, however, are triggered with a differential pulse. The outputs of these delay cells are also differential signals, and they have a substantial DC offset and significant rise and fall times. Because of that, a differential to single ended converter is needed at the output of each replica delay cell. The schematic for the converter is shown in the next figure.

Figure 3.19. Differential to Single Ended Converter.

The converter shown in Figure 3.19 is made up of two opposite phase NMOS differential amplifiers driving two PMOS common source amplifiers connected by an NMOS current mirror. The two levels of amplification are differentially balanced and have a wide bandwidth, which allows the opposing differential input transitions to have an equal delay to the output. The PMOS common source amplifiers convert these to a single

ended signal with 50% duty cycle and steep transitions through the NMOS current mirror. Adding these converters to the output of the replica delay cells loads down the output with additional capacitance, increasing the delay that is observed. If these converters are only used on the replica cells, the delay created by the cells will not agree with (1). In order to mitigate that effect, the differential to single ended converters are also attached to the output of each of the delay cells that make up the VCO, so that they experience the same loading. Doing so gives very good consistency between the overall period of the VCO and the delay of the replica cells.

4. Simulation Results

4.1 PLL Locking

The system is designed in Cadence Virtuoso Analog Design Environment, and simulated using the Spectre simulator. The PLL is simulated to observe locking time and jitter characteristics. The control voltage and VCO frequency are both monitored. Figures 4.1.1 and 4.1.2 show the control voltage and corresponding measured VCO frequency respectively, for the loop reaching its locked state when set to 200MHz. Figures 4.2.1 and 4.2.2 show the same two plots, but with the loop set to operate at 500MHz.

Figure 4.1.1: Control Voltage when set to 200MHz Operating Frequency.

Figure 4.1.2: VCO Frequency when set to 200MHz Operating Frequency.

Figure 4.2.1: Control Voltage when set to 500MHz Operating Frequency.

Figure 4.2.2: VCO Frequency when set to 500MHz Operating Frequency.

As these figures show, the loop took approx. 7 μ s to lock when set to 200MHz, and 3.5 μ s to lock when set to 500MHz. The locking time of the system is most heavily effected by the value K, the divide ratio of the prescaler frequency divider. This is because the value of K that is set determines the effective reference frequency of the system. The reference frequency acts as a clock signal to the PFD, meaning that with a lower reference frequency (larger K value), the *up* and *down* signals will not respond to the changing VCO frequency as rapidly, and the loop will take longer to reach its locked state. In Figure 4.1 the value of K is 4, and in Figure 4.2 the value of K is 2, explaining the larger locking time of Figure 4.2. The effect of the lower reference frequency can also be seen from Figures 4.1.1 and 4.2.1 by looking at the average distance between each instance where the control voltage either increases or decreases, which correspond to the current being sourced or sunk from the charge pump to the loop filter. This occurs about half as frequently in figure 4.1.1, explaining why the locking time is roughly double that of Figure 4.2.1. The largest locking times occur when K is set to 8, which is the maximum value that will be used. An example of this is shown in Figure 4.3, which shows the control voltage when the loop is set to operate at 100MHz.

Figure 4.3: Control Voltage when set to 100MHz Operating Frequency.

The loop takes about 20 μs to reach its locked state in this case, due to the large value of K that is used. Due to the computationally heavy nature of these simulations, they take upwards of 24 hours to run to completion. Because of this, the locking time was not simulated for every VCO frequency. Since the main contributing factor to locking time is known, it can be expected that the locking times for the rest of the VCO frequencies will fall within the range seen here, between 3 μs and 20 μs .

The jitter of the PLL is also studied during these simulations. The measured jitter for four of these simulations is summarized in Table 4. To study jitter, the AC amplitude of the control voltage is measured once the loop has reached its locked state. The voltage is then converted to the delay variation that is seen over each delay cell, by working

backwards from the VCO gain in its linear region to acquire the gain of the delay of a single delay cell. When doing so a gain of 521.25 ps/V is found. The time variations listed in Table 4 therefore correspond to the total error that is possible in the delay of each delay cell.

Table 4: Measured Jitter Characteristics

VCO Frequency (MHz)	Control Voltage Variation (mV)	Time Variation (ps)
200	3.75	1.95
250	1.35	.703
330	1.55	.81
500	2.45	1.27

As the table shows, a very low jitter is observed in this system. Due to the small steps of the delays that are created, however, even a small amount of jitter can still have an effect on system performance. To mitigate the jitter effect, the additional capacitors are added onto the outputs of the bias cell. These capacitors will filter out much of the high frequency AC component of the control voltage. The filtering effect can be seen in Figure 4.4 below, which shows the control voltage and the PMOS bias voltage (the bias voltage that directly controls delay) when set to 330MHz.

Figure 4.4: Control Voltage and PMOS Bias Voltage for 330MHz.

As Figure 4.3 shows, the Vbp signal is a much smoother version of Vctrl, with much less jitter once the loop is locked. The Vbp signal only varies by .15mV from its DC value, as opposed to the 1.55mV of variation seen on the Vctrl signal. This equates to only .16 ps of variation from the nominal value in the delays that are generated.

The full system was simulated as well, to verify the relationship between the VCO output period and the delay seen at each of the replica cells. The results of these simulations are discussed in the next section.

4.2 Delay Generation

To study the delay generation, the full system is simulated. When doing so, the loop must operate until it has reached a locked state, at which point the replica delay cells are triggered. These delay cells are triggered by a differential pulse with a rise and fall time of 100 ps. Figure 4.5 shows the first four of the resulting outputs of the circuit when set to a 100 ps delay, corresponding to a VCO frequency of 500MHz. Figure 4.6 shows these same outputs, but with the delay set to 250 ps, corresponding to a VCO frequency of 200MHz. In Figure 4.5, the trigger pulse is applied at 7.5 μ s, and in Figure 4.6 the trigger pulse is applied at 8 μ s. These values were chosen to allow for enough time for the loop to reach its fully locked state.

Figure 4.5: System Outputs when set to 100 ps Delay.

Figure 4.6: System Outputs When Set to 250 ps Delay.

As the figures shows, uniform delays of 100 ps and 250 ps were observed, respectively, and each of the trigger signals has full swing and a steep transition. These signals are used as the trigger signals for the UWB pulse generators. The error in the delay between each of these signals was also studied for a variety of delay settings. These results are summarized in Table 5 below.

Table 5: Measured Delay of Output Signals and Error

Expected Delay (ps)	Measured Delay (ps)	Error (ps)	Error (%)
100	101	1	1.00
	101.1	1.1	1.10
	101	1	1.00
151.52	152.06	.54	0.36
	152.33	.81	0.53
	151.79	.27	0.18
200	200.16	.16	0.08
	200.26	.26	0.13
	200.15	0.15	0.075
250	250.23	.23	0.09
	251.27	1.27	0.51
	250.94	.94	0.38

The table shows the measured delay between each of the output signals, as well as the difference between that and the expected delay. The maximum error with respect to the delay time observed in the trigger signals is 1.27 ps, when the delay was set to 250 ps. That is a .51% error, which is acceptable for the system. The highest percentage error that was observed was 1.1%, when the delay was set to 100 ps. The percentage here is so high due to the small value of the delay that is set, and this error is also acceptable. These errors are caused by the slight jitter in the control voltage, and agree with the predicted time errors from Table 4.

4.3 Power Consumption

During circuit simulations, the current drawn from the 1.8V power supply is monitored, in order to study the total power consumed by the system. The current waveform for a simulation where the loop is set to oscillate at 200 MHz is shown in Figure 4.6 below.

Figure 4.7: Power Supply Current.

The current draw from the power supply has a maximum value of 3.8mA. Due to the large high frequency variation in the supply current, it is useful to look at the average value instead. A moving average filter with a length of 5000 is applied to the current waveform in MATLAB, and the resulting current waveform is shown below.

Figure 4.8: Average Power Supply Current.

As the figure shows, the average current draw of the beamforming subsystem is quite low once the loop is in its locked condition. It has an average value of only 665uA. Combining that result with the power supply voltage of 1.8V using the standard power equation leads to an average power consumption of 1.2 mW once the loop is locked.

5. Beamforming

5.1 Theoretical Equations

The beamforming capabilities of a true time delay phased array system depend on two main parameters, the time delay between each successive antenna element, Δ , and the distance these elements are spaced, d . The relationship between the delay Δ and the relative beam angle for a true time delay phased array system can be characterized as

$$\Delta = d * \frac{\sin \theta}{c} \quad (5.1)$$

which leads to a scanned angle of

$$\theta = \sin^{-1} \frac{\Delta * c}{d} \quad (5.2)$$

The overall beam pattern created by the phased array system can be formed by combining the complex voltage waveforms that are generated by each radiating element, while also taking into account the linear position of each element in the array. For an array of M elements, the position can be denoted by

$$x_m = (m - 0.5(M + 1)) * d, m = 1, \dots, M \quad (5.3)$$

The spatial response of the array at an angle θ incident to the array, known as the array factor (AF), can then be represented by

$$AF = \sum_{m=1}^M A_m e^{j\frac{2\pi}{\lambda}x_m \sin \theta} \quad (5.4)$$

where A_m represents the complex voltage applied to each radiating element [1]. By substituting the expression for complex voltage into Equation (5.4), the following equation can be obtained for the array factor at the angle θ ,

$$AF = \sum_{m=1}^M a_m e^{j\theta_m} e^{j\frac{2\pi}{\lambda}x_m \sin \theta} \quad (5.5)$$

Equation (5.5) is maximized at a particular value of $\theta = \theta_0$ when the phase offset of each element, θ_m , satisfies

$$\theta_m = -\frac{2\pi}{\lambda}x_m \sin \theta_0 \quad (5.6)$$

Equation (5.6) shows us that by precisely controlling the phase offset of each element, done in this case by controlling the time delay between the radar pulses, it is possible to control where the maximum power of the composite signal is directed [1]. It should also be noted that Equation (5.6) will be satisfied for two values between 0° and 180° , due to the sine function in the equation. This means that there will be two main lobes of the constructed beam, which are symmetric about 90° . The measured beam patterns from [2] also show that this is the case, and it is discussed further in the next section.

It is also possible to use the phase offset of each element that results from Equation (5.6) to calculate the delay required to achieve the desired scan angle. The first step to doing so is to take the difference between two successive elements from the vector that results from Equation (5.6).

$$\theta_{dif} = \theta_m - \theta_{m-1} \quad (5.7)$$

The result of Equation (5.7) must then be converted from radians to a percentage of the total period, as follows.

$$p = \frac{\theta_{dif}}{2\pi} \quad (5.8)$$

Once the percentage is calculated, all that is needed is the period of the radar signal that will be applied. In this system, a 1 GHz pulse will be used, resulting in a period of 1ns. Multiply the result of Equation (5.8) by 1ns, and the result is the delay required between each successive element. When these calculations are done, the results agree with the results of Equation (5.1) for all desired scan angles, giving good confidence in these equations.

Equation (5.5) also gives us an expression that allows us to plot the overall shape of the beam formed by the array, for any desired angle[1]. It is plotted in MATLAB, which demonstrates how changing different parameters will affect the array factor. One

Parameter that has a large effect on the array factor is the number of antenna elements that are used. Figure 5.1 show the resulting beam patterns for a 10 element and 30 element array.

Figure 5.1: Array Factor for 10 Element and 30 Element Arrays set to 30 Degrees (Delay of 300 ps).

As the figure shows, using a larger number of antenna elements results in a smaller 3db beamwidth, with a value of 10° for a 10 element array and 3.25° for a 30 element array. Using more antennas also results in more side lobes, but with less power in the side lobes. These characteristics translate to better performance of a phased array system using more antennas, so there is a trade-off between system performance and array size. Using more antennas also results in needing more replica delay cells in the beamforming subsystem, resulting in larger chip size and power consumption. The beam patterns are shown for the particular system described in the next section.

5.2 Theoretical Performance of this System

In this system, the time delays generated range from 100 ps to 500 ps in 25 ps

increments, and an antenna spacing of 18cm is used. These values gives the desired angle range of 9.6° to 56.4° , with 2.75° angle resolution based on Equation (5.5). The delays and respective scan angles that the system can achieve are shown in Figure 5.2 below.

Figure 5.2: Delays and Resulting Scan Angles.

In this project, an array of 10 antennas is used. The number of antennas is chosen to achieve a 10° -3dB beam width, based on Equation (5.5). The resulting beam pattern for a 10 element array spaced 18cm apart with a delay of 200 ps is shown in Figure 5.3.

Figure 5.3: Beam Pattern of Array Used with 200 ps Delay.

Using a 200 ps delay will result in a beam angle of 19.4 degrees, as the figure shows. The figure also demonstrates that with the array specifications that will be used, there will be about -12dB of power in the first side lobe. Another useful way to visualize the beam pattern is by plotting the magnitude of the array factor in polar coordinates. Plotting these is done for all scan angles in Figure 5.4 below.

Figure 5.4: Beam Patterns Achieved.

The figure simulates the beam patterns that are achievable using the array as described. The antenna array is oriented along the horizontal axis of the figure. As the figure shows, the region ranging from 9.6° to 56.4° is covered very well by the beam patterns that will be created. This means that the radar system will have good image resolution. Figure 5.4 also shows that there will be two main lobes created for every delay that is set, which are symmetric about 90° , a result of Equation (5.6). The two main lobes are also demonstrated in Figure 5.5, which shows the array factor when the array is set to a 500 ps delay, corresponding to a scan angle of 56.4° . Here the second main lobe is directed at 123.6° .

Figure 5.5: Beam Pattern for 500 ps Delay.

Even though there are two main lobes created, as Figure 5.5 shows, the performance of the system will not be affected. That is because the array is oriented in a way such that these undesired beams will be traveling horizontal to the ground, so they will not reflect back to the receiver antennas within the time required for them to be accounted into the image.

6. Circuit Layout

This section discusses the CMOS process technology that will be used to fabricate the system. It also discusses the design process that is followed when creating the layout of the system. Finally it presents the final design layout and some associated metrics.

6.1 Process Technology

The circuit will be fabricated using Global Foundries 7HV .18 μ m CMOS process technology. It is a mixed supply technology, containing transistors that are capable of accepting supply voltages from 1.8V all the way up to 50V. Using this technology allows the high voltage pulse generators to be contained on the same IC as the low voltage control circuitry. The control circuitry is created with the 1.8V CMOS devices. These devices have a minimum channel width of 220nm. Due to the complications associated with making source and drain connections to these small channels, a minimum width of 500nm was used for the devices in the design. The minimum channel length of 180nm was used for most of the devices in this design.

6.2 Layout Design

When constructing the circuit layout, first the basic logic gates were designed, as these are the building blocks for many of the digital portions of the circuit. The layout of the digital logic gates is shown below.

Figure 6.1: Inverter Layout.

Figure 6.2: 2 input NAND Gate Layout.

Figure 6.3: 3 Input NAND Gate Layout.

Figure 6.4: 4 Input NAND Gate Layout.

Figure 6.5: NOR Gate Layout.

As Figures 6.1 through 6.5 show, these logic gates are designed in the traditional fashion. This includes placing the power rail along the top of the layout, and the ground rail towards the bottom. The power and ground rails are spaced $4.86\mu\text{m}$ apart in all of these layouts, to allow for easy integration of large numbers of these cells. The input and output rails are also along the bottom of the layout, as doing so facilitates smooth integration as well. All of the logic gates were constructed with minimum size transistors, to reduce size as well as power consumption. Once these basic gates are constructed, they are used as the building blocks for the rest of the digital portions of the circuit, such as the exclusive OR gate shown in Figure 6.6, which is made up of 4 2 input

NAND gates, and the D flip-flop shown in Figure 6.7, which is made up of 6 3 input NAND gates.

Figure 6.6: XOR Gate Layout.

Figure 6.7: D Flip-Flop Layout.

The design method described is continued through to the higher level digital components, such as the 3-bit counter, 3-bit comparator, and T flip-flop, shown in the next three figures.

Figure 6.8: 3-Bit Counter Layout.

Figure 6.9: 3-Bit Comparator Layout.

Figure 6.10: T Flip-Flop Layout.

The three components shown in Figures 6.8 through 6.10 were then combined to create the prescaler frequency divider, shown in Figure 6.11 below.

Figure 6.11: Prescaler Frequency Divider Layout.

In a similar design fashion, the D latch is created using the basic logic gates. The D latch is then used, along with other logic gates, to create the divide by 2/3 element. Five of these divide by 2/3 elements are then combined to create the multi-modulus in loop frequency divider. These layouts are shown in the next three figures.

Figure 6.12: D Latch Layout.

Figure 6.13: Divide by 2/3 Frequency Divider Layout.

Figure 6.14: Multi-Modulus Frequency Divider Layout.

The final digital component is the phase-frequency detector, which is shown in Figure 6.15.

Figure 6.15: Phase Frequency Detector Layout.

Once the digital portion of the circuit was fully designed, it came time to create the layout for the analog components. When creating these components, minimum transistor size is not always used. Larger gates are used to allow for proper current flow in the charge pump circuit, which is shown in Figure 6.16.

Figure 6.16: Charge Pump Layout.

The remainder of the analog components are shown in the next three figures. These include the delay cell, the bias generator, and the differential to single converter.

Figure 6.17: Differential Delay Cell Layout.

Figure 6.18: Differential to Single Converter Layout.

Figure 6.19: Bias Generator Layout.

A large resistor was initially used in the bias generator schematic. The resistor caused this cell to take up an extremely large amount of chip space, which is not economical, and

therefore was not desirable. The resistor has since been replaced with a PMOS transistor, as Figure 6.19 shows. The new transistor was sized properly so that it accurately mimics the large resistor, therefore not affecting the circuit operation.

Figure 6.20: Full System Layout.

The full circuit layout is shown in Figure 6.20. As the figure shows, the majority of the chip area is taken up by the four capacitors that are used. These devices are inherently large, but they are required for system stability, so they cannot be removed from the design.

Figure 6.21: Passing DRC Results

Figure 6.21 shows the results of a design rule check (DRC) that was performed on the full layout. DRC checks to ensure that all process design rules have been followed during the creation of the layout. As the figure shows, no violations of the design rules for this process were detected. The only things that show up as results are for informational purposes. If there were any rule violations in the design, they would show up here as errors. The DRC passing indicates that the layout was designed properly, and can be successfully fabricated using the process technology.

Figure 6.22: Passing LVS Results

Figure 6.22 shows the results of the layout versus schematic (LVS) check that was performed on the layout. LVS compares all of the components, pins, nets, and interconnections that are present in the schematic to those created in the layout, to ensure that they all match. Passing results indicate that the layout created is actually an accurate representation of the schematic it is trying to replicate. As the figure shows, the layout created matches the schematic exactly. The next section discusses metrics related to the layout.

6.3 Layout Metrics

The full system layout takes up a total chip area of $.049\text{mm}^2$. It uses a total of 1233 transistors, 1 resistor, and 4 capacitors. Metal layers 1 and 2 are used in the design of the individual components. Metal layers 3 and 4 are used to make interconnections between these components, and metal layers 5 and 6 are used to create the MIM (metal insulator metal) capacitors.

7. Conclusions

7.1 Success of this Project

A single chip beamforming system has been designed using Global Foundries 7HV $.18\mu\text{m}$ high voltage CMOS process. The controls operate at low supply voltage of 1.8V, while the system is also capable of generating high voltage GPR pulses. The power consumption of the control system is low ($<1\text{mW}$). Simulations show that the system can

generate delays that vary from 100 ps to 500 ps in 25 ps increments. The corresponding beam angles range from 9.6° to 56.4° in steps of 2.75° . The UWB output pulses from the chip have amplitude of 20V and pulse width of 2ns, making the system well suited for GPR. Because of that, there is no need for off chip power amplifiers, making it a single chip solution.

7.2 Future Work

The next step in the project is to fabricate the beamforming system onto a chip, so that it can be tested to verify its functionality. Once the chip is fabricated, it will be installed onto a custom breakout printed circuit board (PCB), so that it can be tested. The PCB will contain switches that can be used to set the control inputs of the frequency divider. The chip will be fed a 1.8V supply. The control voltage will be monitored with an oscilloscope from the time when power is applied to the chip. The frequency of the VCO will also be monitored, using a signal analyzer. Once the loop has locked, it will be fed a differential trigger pulse, also with amplitude of 1.8V. The ten trigger outputs will be monitored with an oscilloscope, and the delay between the rising edges of each signal will be measured. The measurement will be done for every delay setting. The locking times will be measured and recorded as well, as these will determine the frequency at which the different beam angles can be cycled. Power consumption of the chip will also be measured, purely as a metric.

Once it has been verified that the beamforming system is generating proper delays, it will be time to integrate the beamforming circuitry with the rest of the phased array GPR system into one chip layout. That layout will include the high voltage pulse generators, as well as the receiving circuitry required by the radar system. The chip will then be fabricated, so that the full system may be tested. To test the full system, the chip will again need to be installed onto a breakout PCB. The PCB will have connections for the 10 antenna elements of the array, as well as a way to interface with the control signals of the programmable PLL. It will also have a data output so that the measured images can be studied. To increase ease of use, a simple Verilog HDL script can be written that would allow the user to input the desired scan angle, and would set the control inputs of the two frequency dividers correspondingly. The table in Appendix A outlines what values will need to be set for each individual scan angle.

Once the setup is complete, the first thing to measure is the beam radiation patterns created by the system. These measured patterns will be compared with the expected beam patterns, and if there are any slight differences, they will be noted. These can be used to calibrate the system, and will be accounted for in the code that generates the reconstructed image. Once the calibration is complete, the final test will be a full functional test of the phased array GPR system.

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Appendix A

Scan Angle Desired	K Value Needed	Control 0 Bits			N Value Needed	Control 1 Bits				
		Bit 0	Bit 1	Bit 2		Bit 0	Bit 1	Bit 2	Bit 3	Bit 4
9.59	2	1	0	0	50	0	1	0	0	1
12.02	2	1	0	0	40	0	0	0	1	0
14.63	2	1	0	0	33	1	0	0	0	0
17.00	4	0	1	0	57	1	0	0	1	1
19.47	4	0	1	0	50	0	1	0	0	1
22.26	4	0	1	0	44	0	0	1	1	0
24.62	4	0	1	0	40	0	0	0	1	0
27.58	4	0	1	0	36	0	0	1	0	0
30.00	6	1	1	0	50	0	1	0	0	1
32.92	6	1	1	0	46	0	1	1	1	0
35.55	6	1	1	0	43	1	1	0	1	0
38.68	6	1	1	0	40	0	0	0	1	0
41.81	8	0	0	1	50	0	1	0	0	1
45.17	8	0	0	1	47	1	1	1	1	0
49.25	8	0	0	1	44	0	0	1	1	0
52.53	8	0	0	1	42	0	1	0	1	0
56.44	8	0	0	1	40	0	0	0	1	0